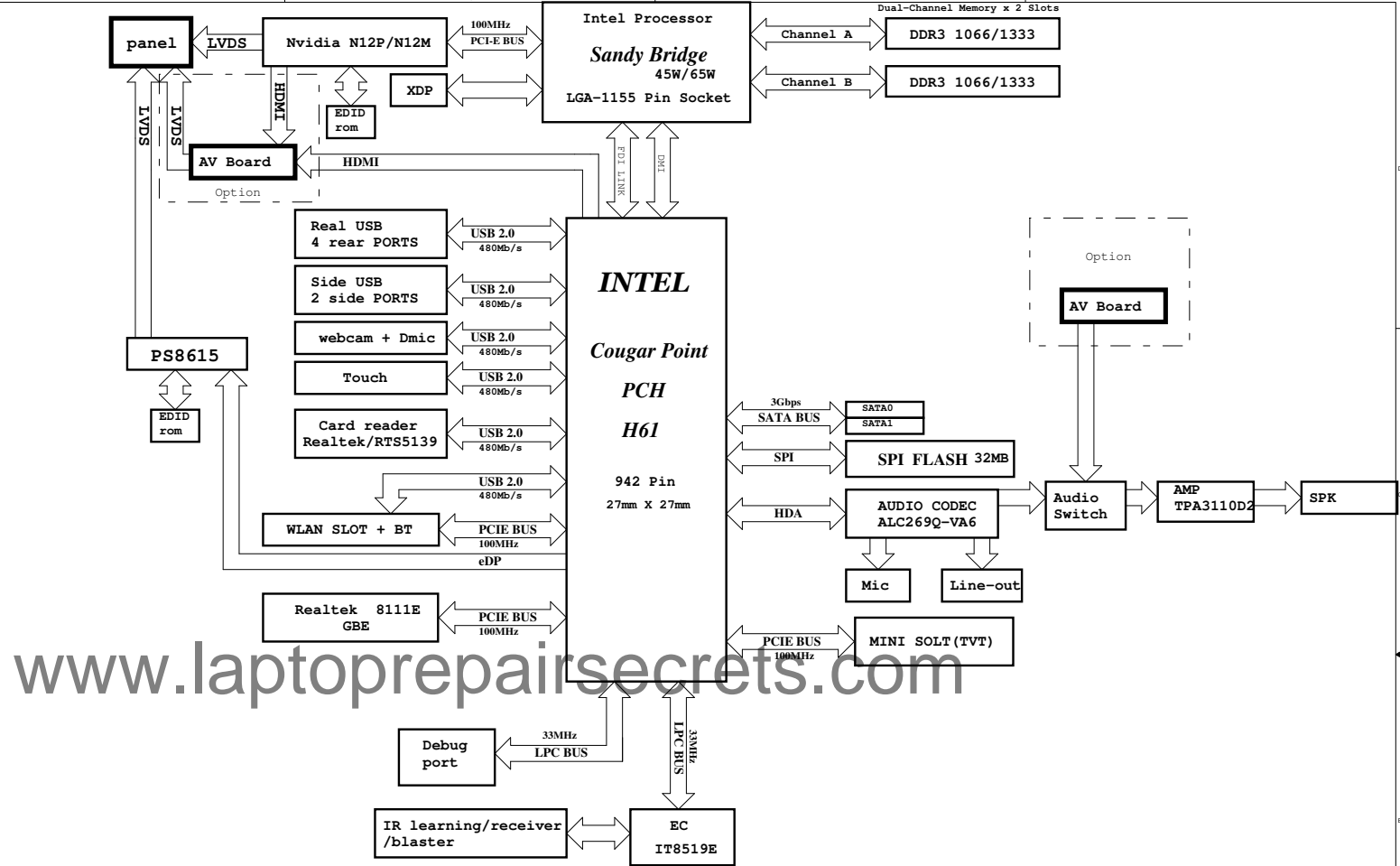
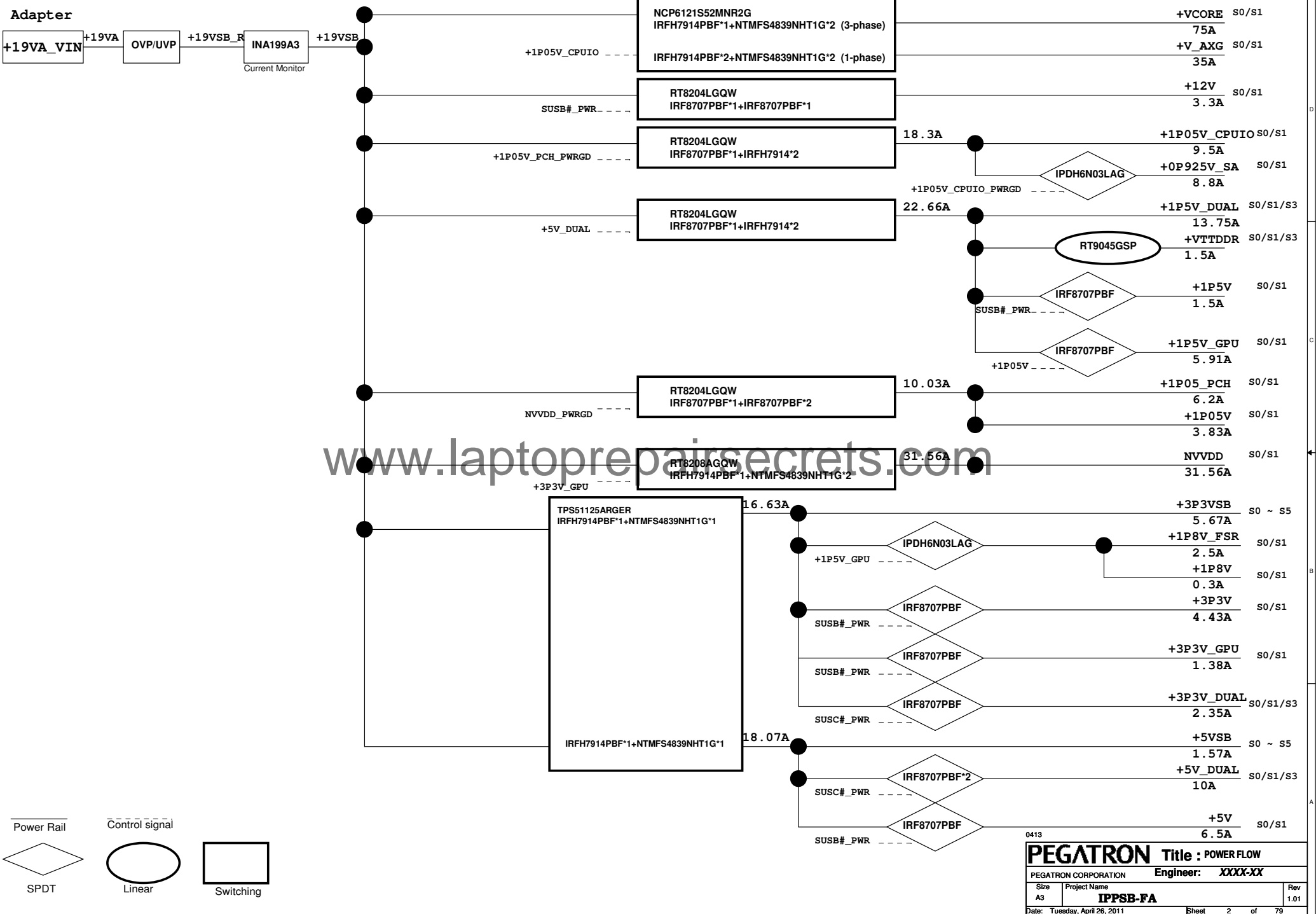


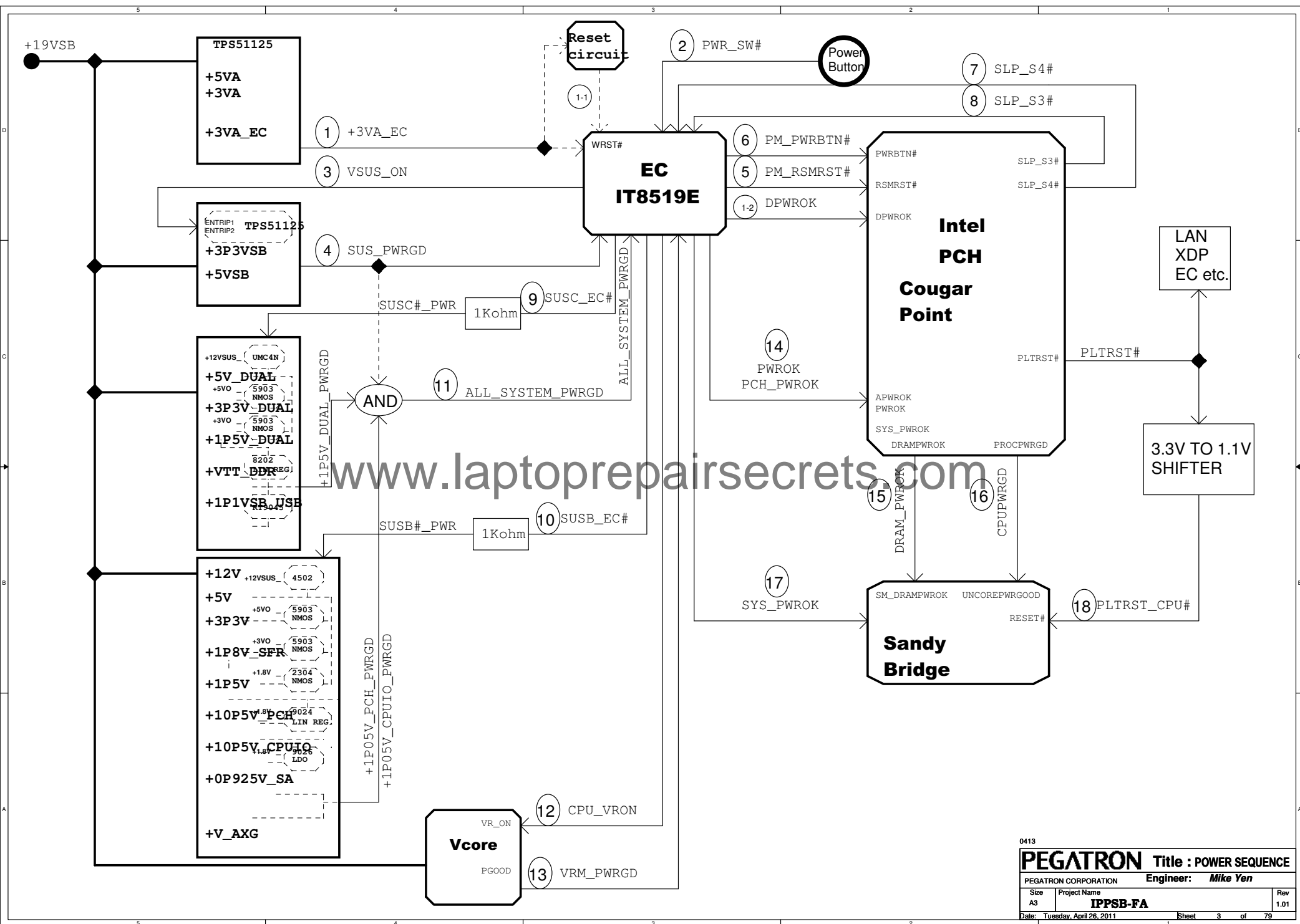
IPPSB-FA

PAGE	TITLE
01	BLOCK DIAGRAM
02	POWER FLOW
03	POWER SEQUENCE
04-09	CPU LGA1155 DDR3 A 1-6
10	DDR3 CHANNEL A G/F
11	DDR3 CHANNEL B G/F
12	DDR3 TERMINATION A&B
13	PLTRST_CPU# & SMBus
14	Converter Controller
15-16	LVDS&AV CONN
17-25	INTEL PCH 1-9
27-28	LAN
29-30	CODEC&CONN
31-32	AMP&SWITCH
33-35	USB&HUB&BT
36	HPD DET
37-38	MINI CARD (WL&TVT&DMC)
39	Misc. conn&Touch&Wcam&RTC
40	FAN
41	PWR LED & Button*
42	IR LEDs
43-44	EC 8519
45	SM BUS & SPI ROM
46	SCREW HOLE
47	UVP, OVP & +19VSB
48	LOAD SWITCH
49	+3P3VSB&+5VSB
50	+1P5V_DUAL & +1P2V
51	Current Monitor
52	+12V & +1P8V
53	+1P05V_CPUIO&+0P925V_SA
54	POWER_PROTECT
55	+1P05V_CPUIO CAP
56	+VTT_DDR
57	+V_AXG DRIVER
58	+VCORE CONTROLLER
59-61	+VCORE CAP
62	+1P05V&+1P05V_PCH
63-64	CPU&PCH XDP DEBUG CONNECTOR
65	VGA CONN
66-67	GPU DDR3
68	VGA-N12P_STRAPPING+EEPROM
69	MXM.VGA-N12P_Xtal/Thermal
70-71	GPU HDMI (DMC&AV)
72	GPU CTRL
73	GPU.VGA_N12P_PCI-E I/F
74	GPU PCI-E LVDS_VGA
75	MXM.GPU Discharge
76	GPU_POWER&GND
77	MXM.NVVD
78	Card Reader RTS5139-GR
79	EDP CH7511

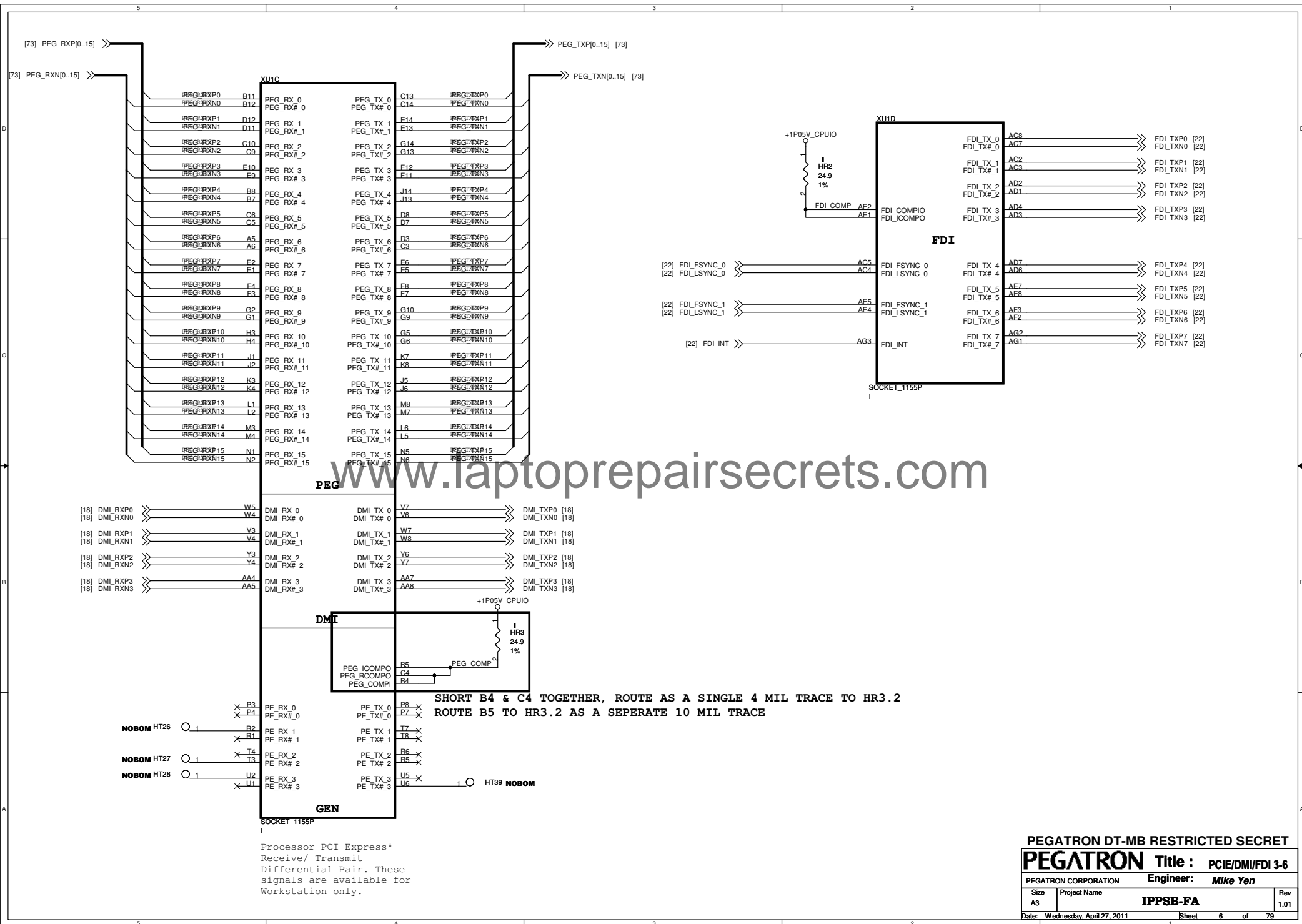




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0413



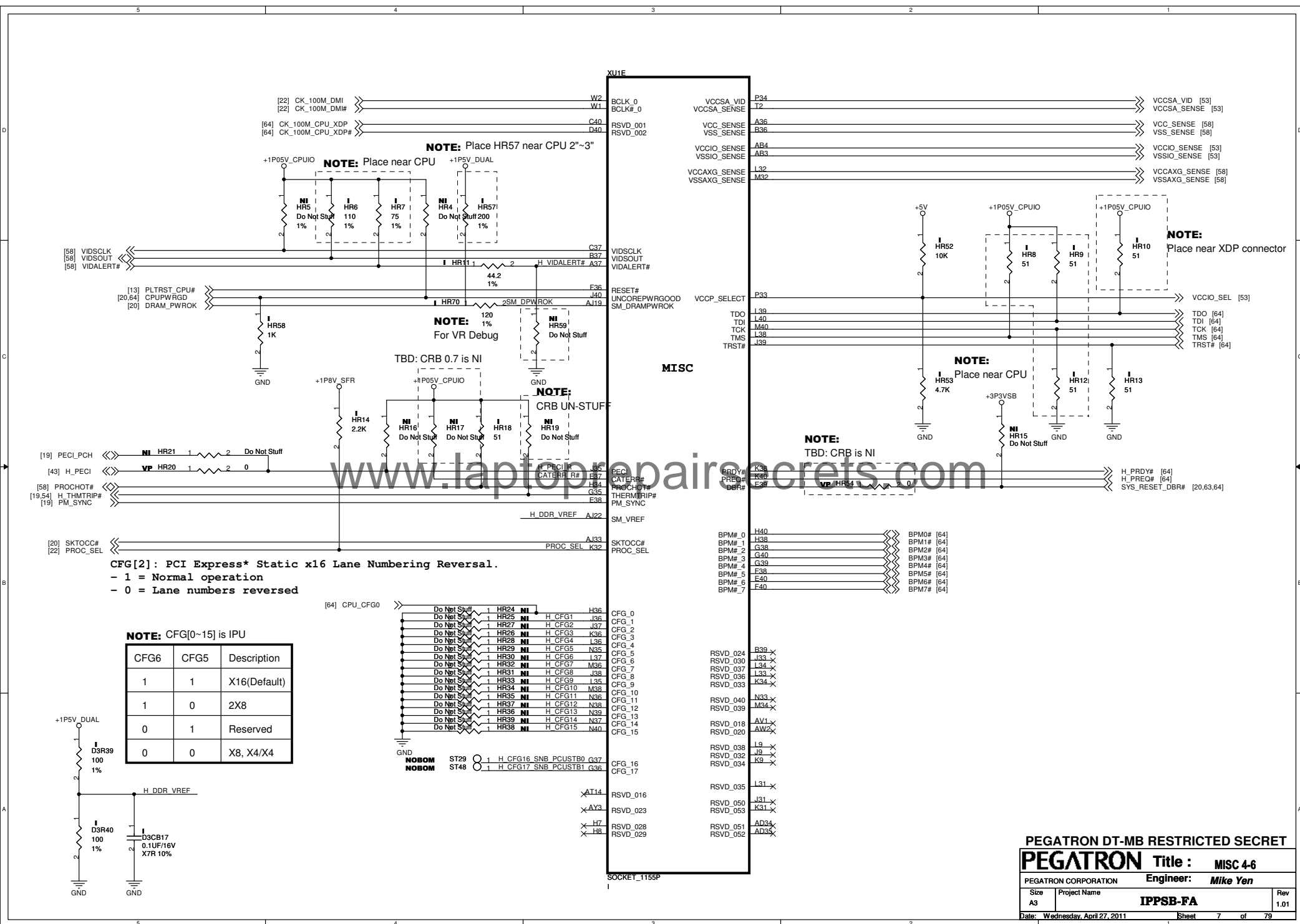
PEGATRON DT-MB RESTRICTED SECRET

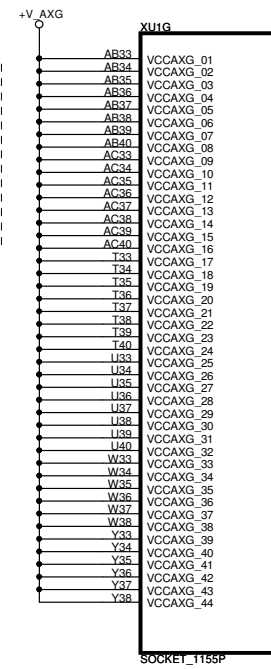
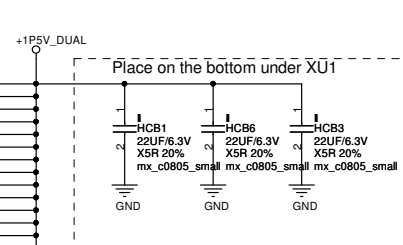
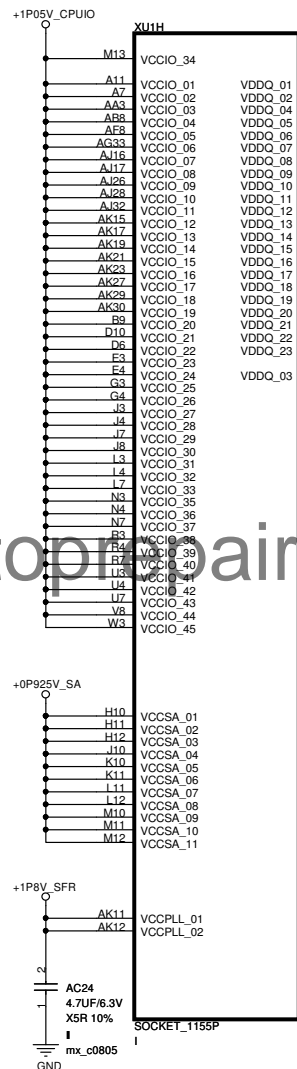
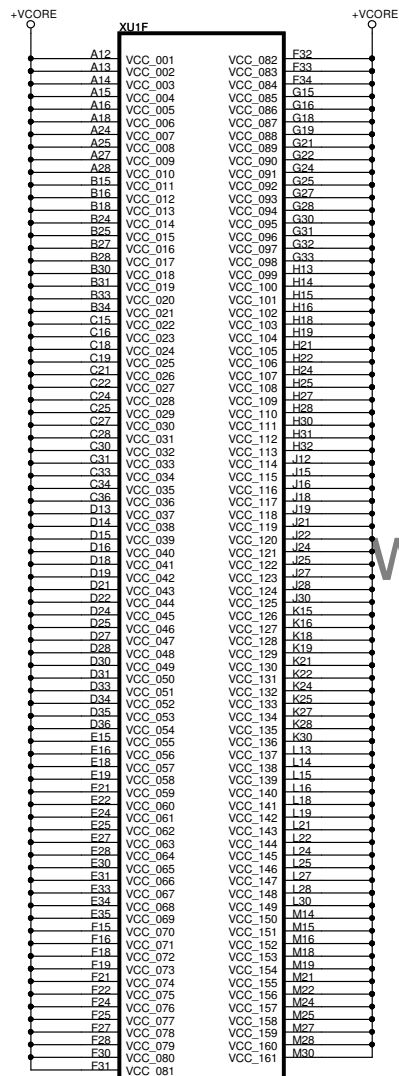
PEGATRON Title : PCIE/DMI/FDI 3-6

PEGATRON CORPORATION Engineer: Mike Yen

Size A3 Project Name IPPSB-FA Rev 1.01

Date: Wednesday, April 27, 2011 Sheet 6 of 79





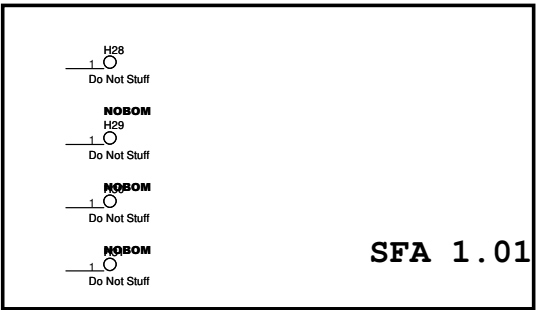
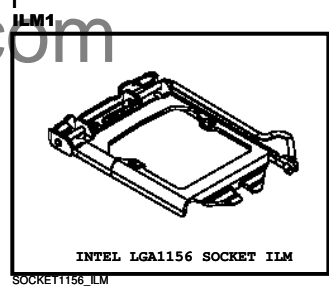
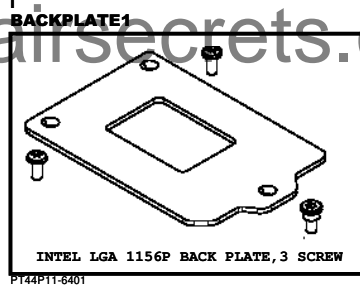
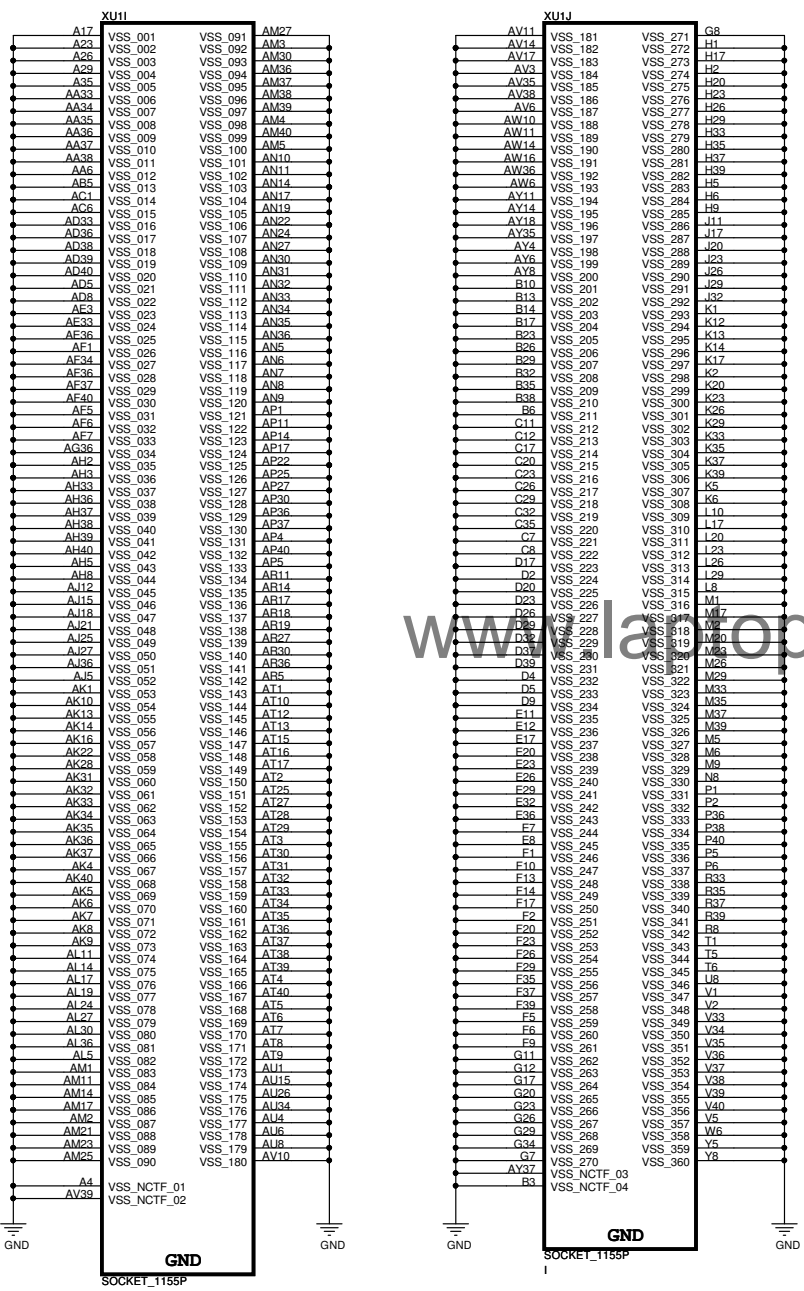
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VCC 5 - 6

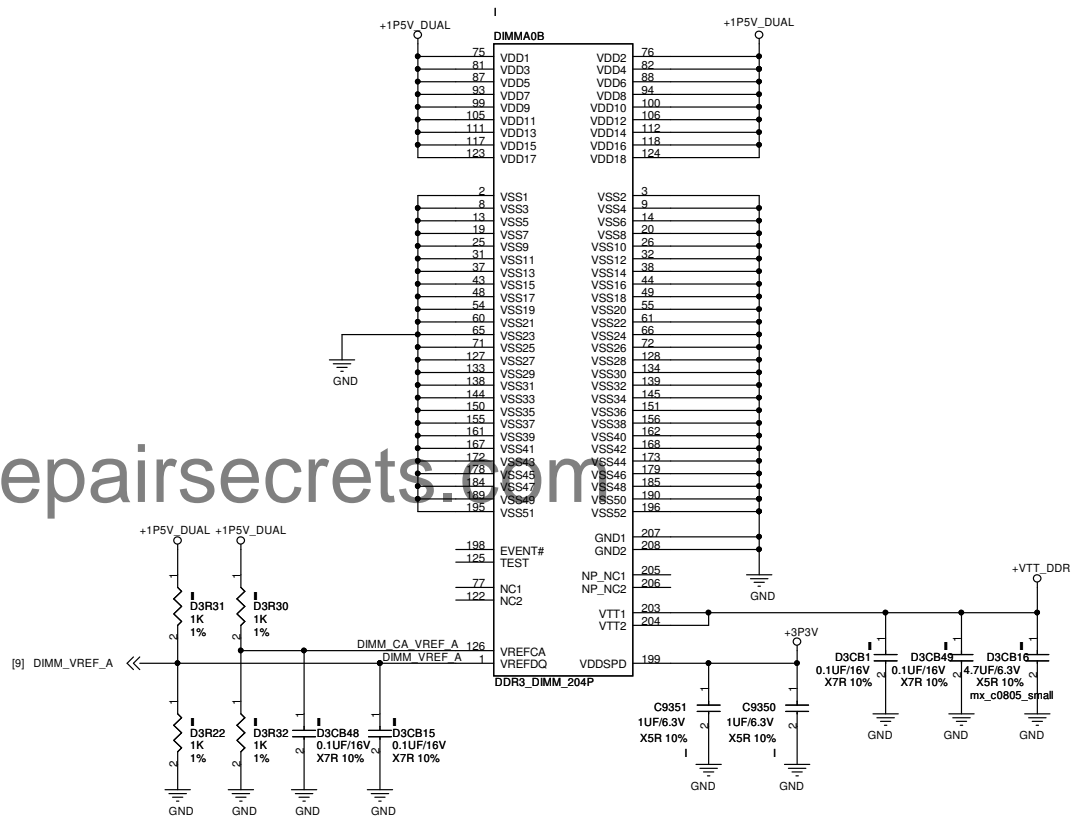
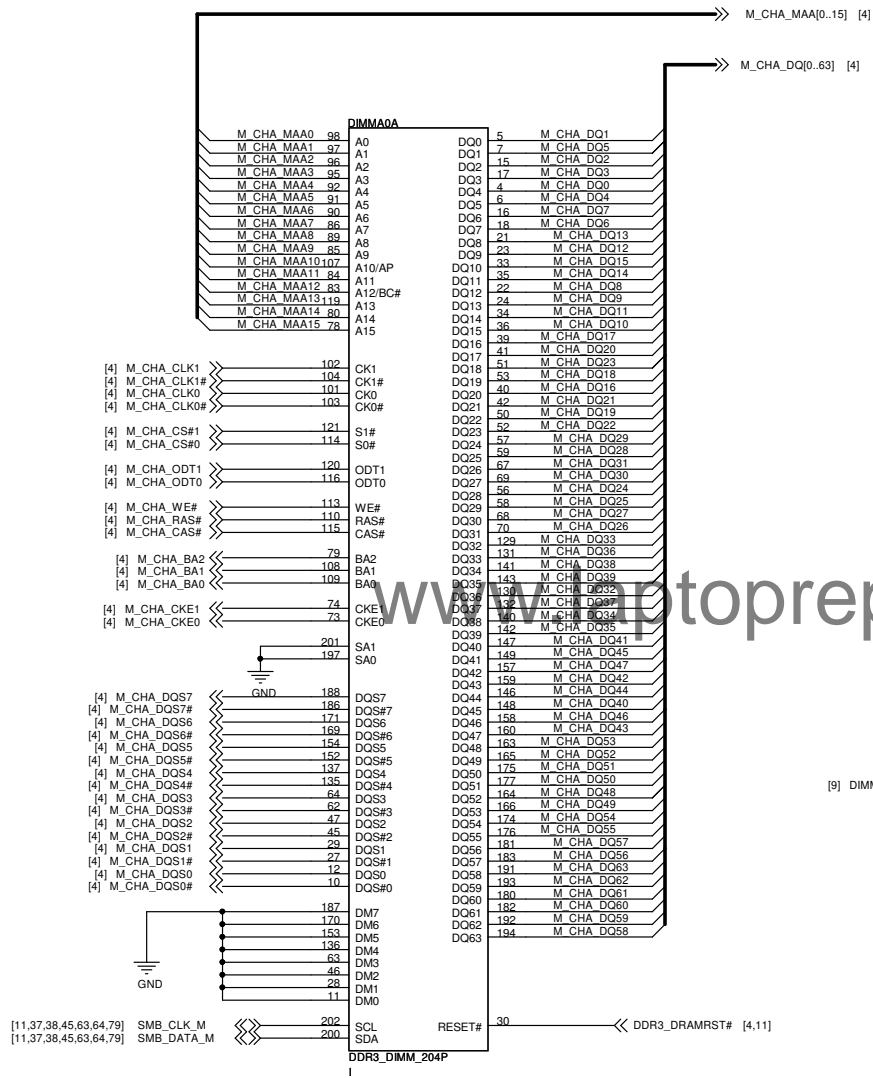
PEGATRON CORPORATION Engineer: Mike Yen

Size A3 Project Name IPPSB-FA Rev 1.01

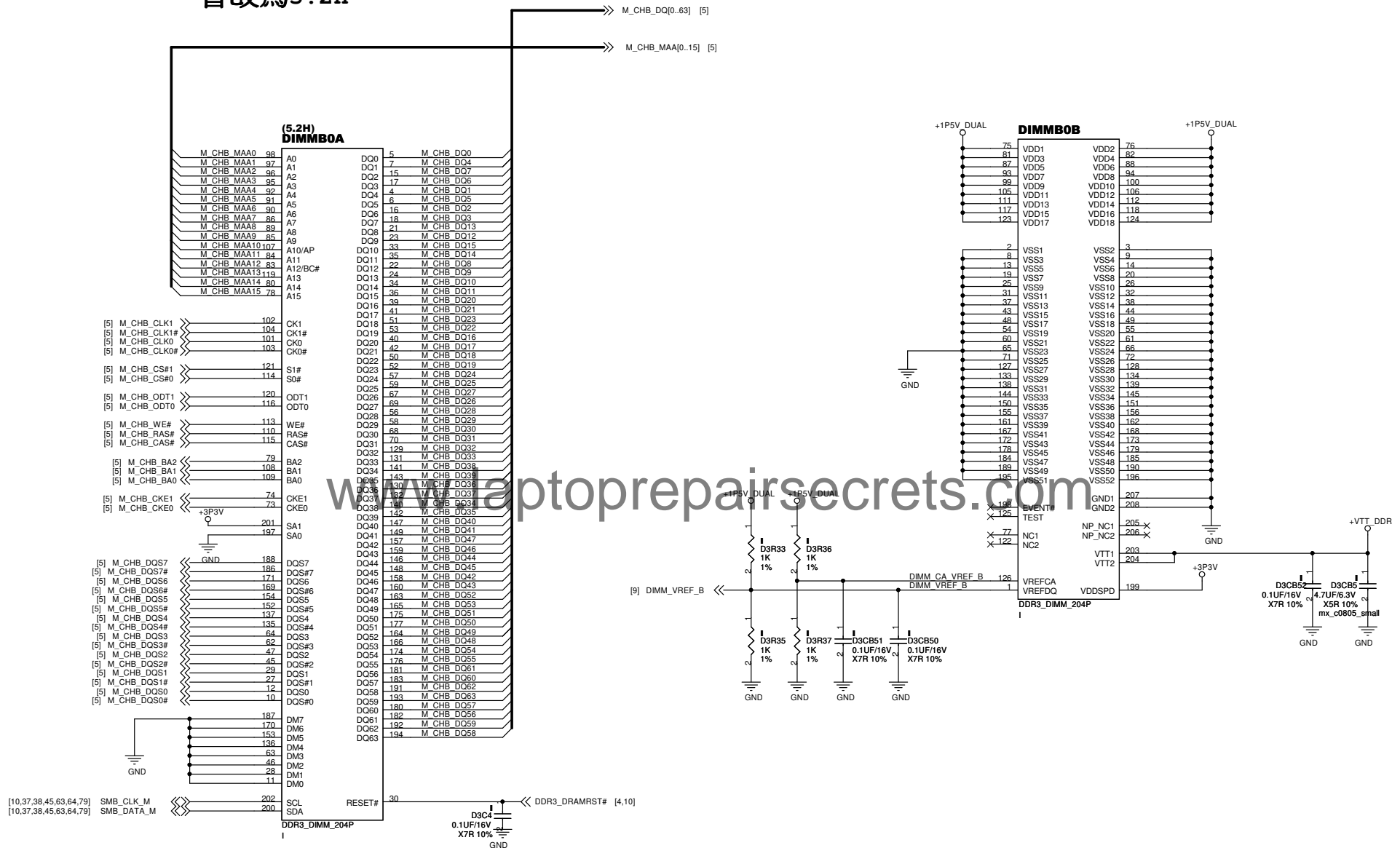
Date: Tuesday, April 26, 2011 Sheet 8 of 79

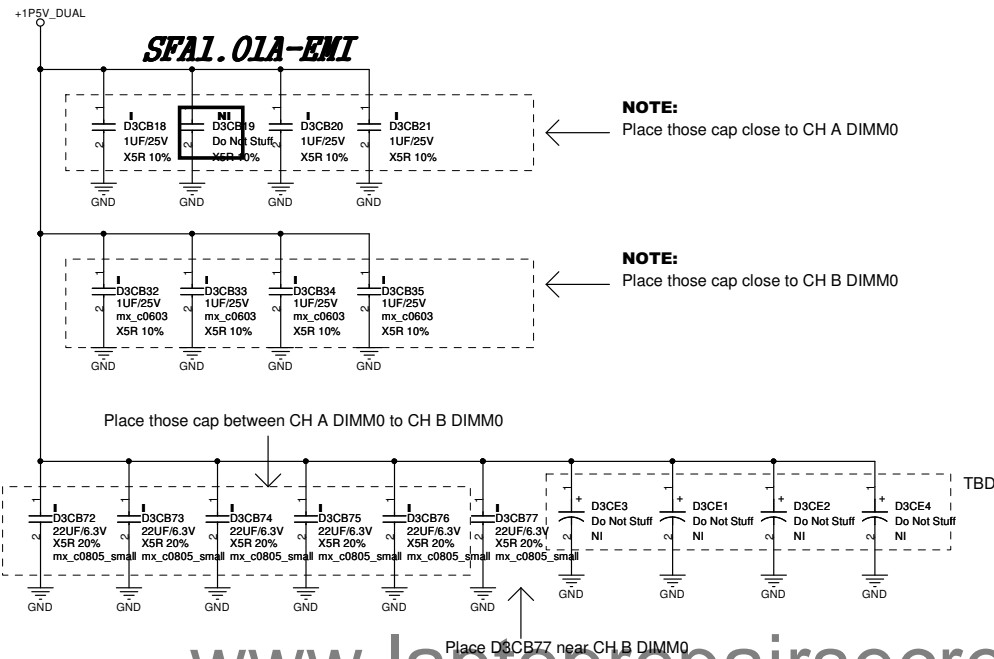


皆改爲5.2H



皆改爲5.2H

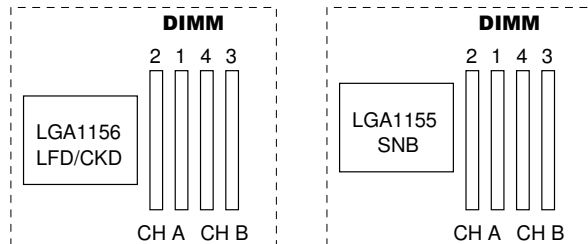




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NOTE:

DIMM Placement for different platform



PEGATRON DT-MB RESTRICTED SECRET

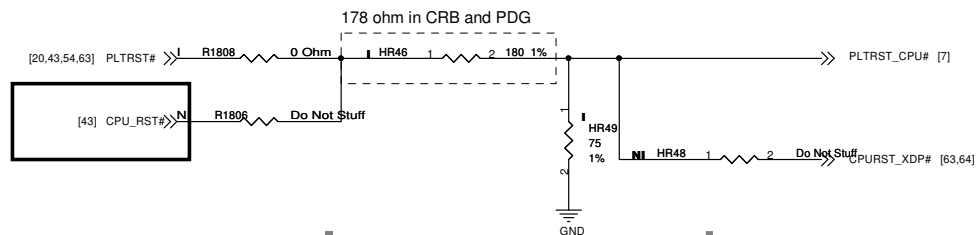
PEGATRON Title : DDR3 TERMINATION A&B

PEGATRON CORPORATION Engineer: **Mike Yen**

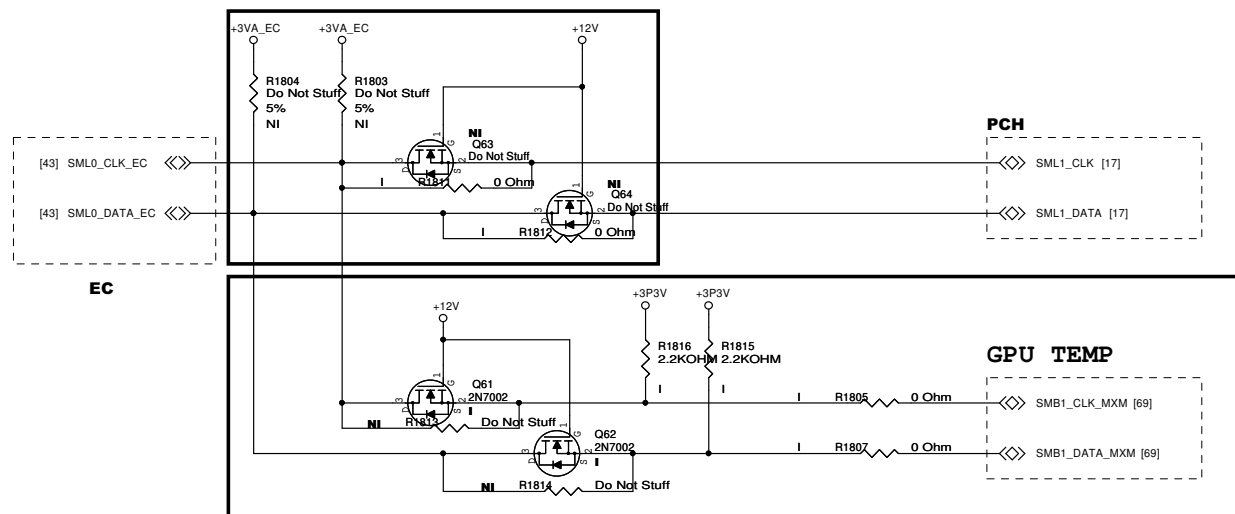
Size A3 Project Name **IPPSB-FA** Rev 1.01

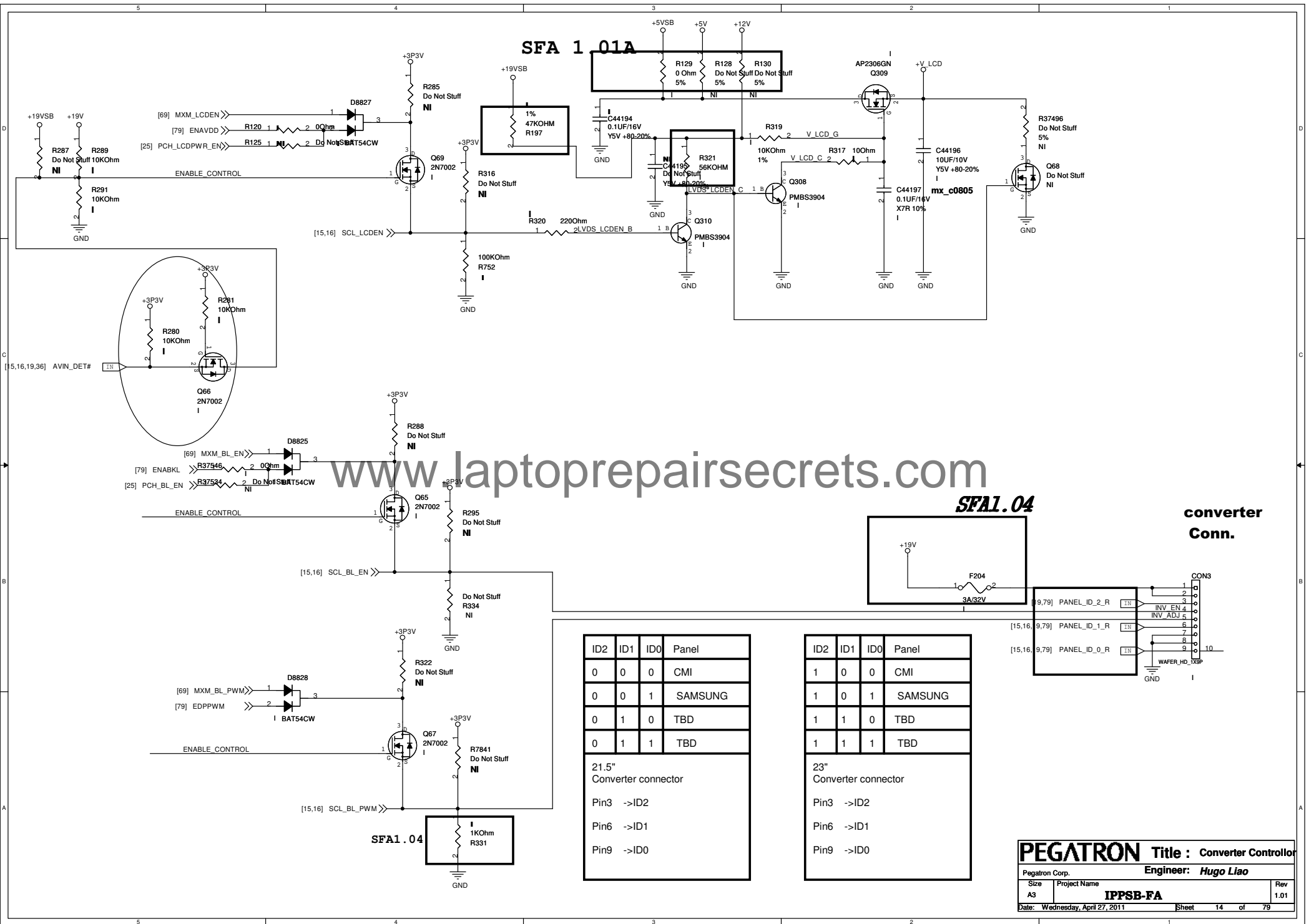
Date: Tuesday, April 26, 2011 Sheet 12 of 79

PLTRST_CPU#



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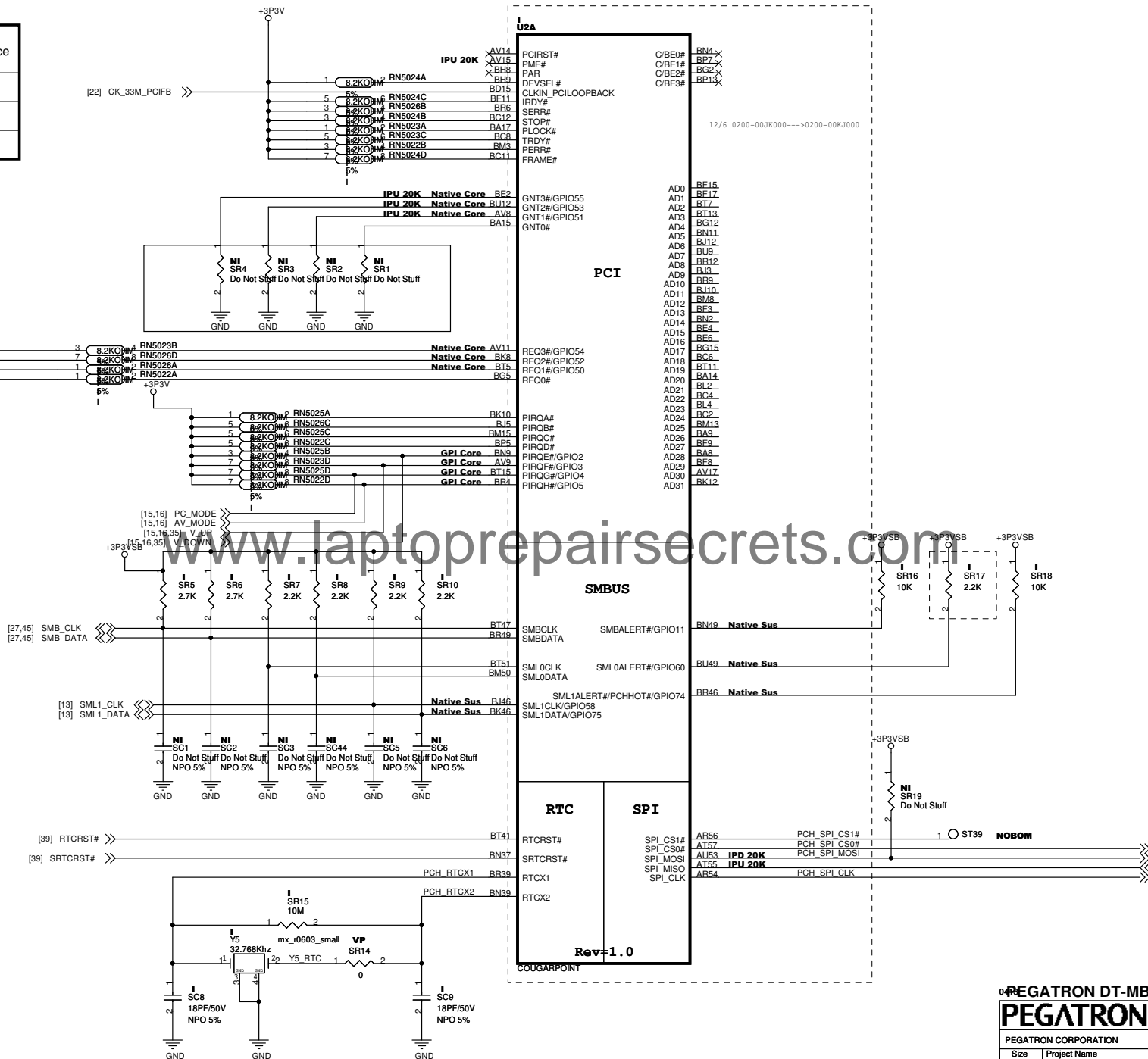




NOTE: Strapping Options Flash

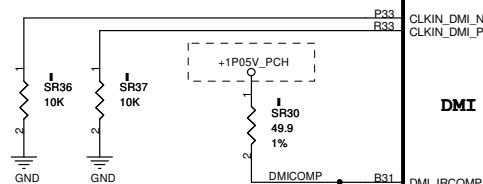
GNT1#	SATA1GP /GPIO19	Boot Device
0	0	LPC
1	0	PCI
1	1	SPI

I2C/en(dis)able/S3
for accelerometer



NOTE:

Used for for DMI, PCIe(Pcie 2.0 jitter spec compliant).

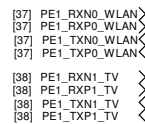
**NOTE:**

trace length < 450 mils

WLAN

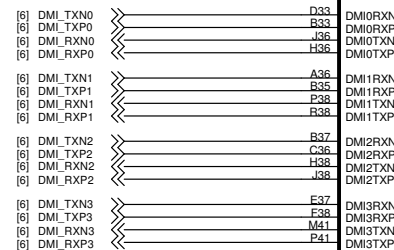
TVT

LAN



NOBOM	ST16	1	TP	PCH	RN7	H12
NOBOM	ST14	1	TP	PCH	RP7	H12
NOBOM	ST13	1	TP	PCH	TN7	E15
NOBOM	ST15	1	TP	PCH	TP7	F13
NOBOM	ST9	1	TP	PCH	RN8	H10
NOBOM	ST10	1	TP	PCH	RP8	J10
NOBOM	ST11	1	TP	PCH	TN8	B13
NOBOM	ST12	1	TP	PCH	TP8	D13

for H61,
PCIe ports 7 and 8 are disabled.

U2B**DMI**

DMI_IRCOMP
DMI_ZCOMP

DMI2RBIAS

PCIe

PERn1
PERp1
PETn1
PETp1

PERn2
PERp2
PETn2
PETp2

PERn3
PERp3
PETn3
PETp3

PERn4
PERp4
PETn4
PETp4

PERn5
PERp5
PETn5
PETp5

PERn6
PERp6
PETn6
PETp6

PERn7
PERp7
PETn7
PETp7

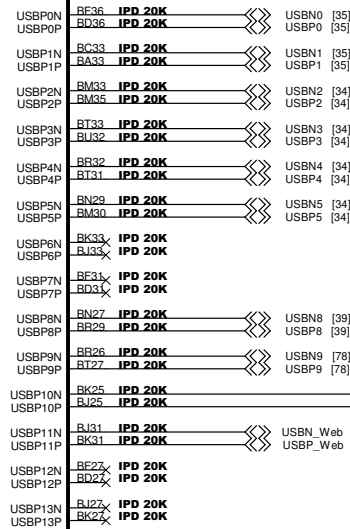
PERn8
PERp8
PETn8
PETp8

COUGARPOINT**USB**

OC0#/GPIO53
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO9
OC6#/GPIO10
OC7#/GPIO14

CLKIN_DOT_96N
CLKIN_DOT_96P

USBRBIAS#
USBRBIAS



side x2 #1 USB Debug port

Rear x4

Touch Panel

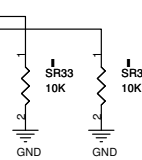
CARD READER

#9 USB Debug port

Web Can

NOTE:

Used for integrated graphics, generate USB backbone,
24MHz HDA bit, and 48MHz clock.

**NOTE:**

trace length < 200 mils

PEGATRON DT-MB RESTRICTED SECRET

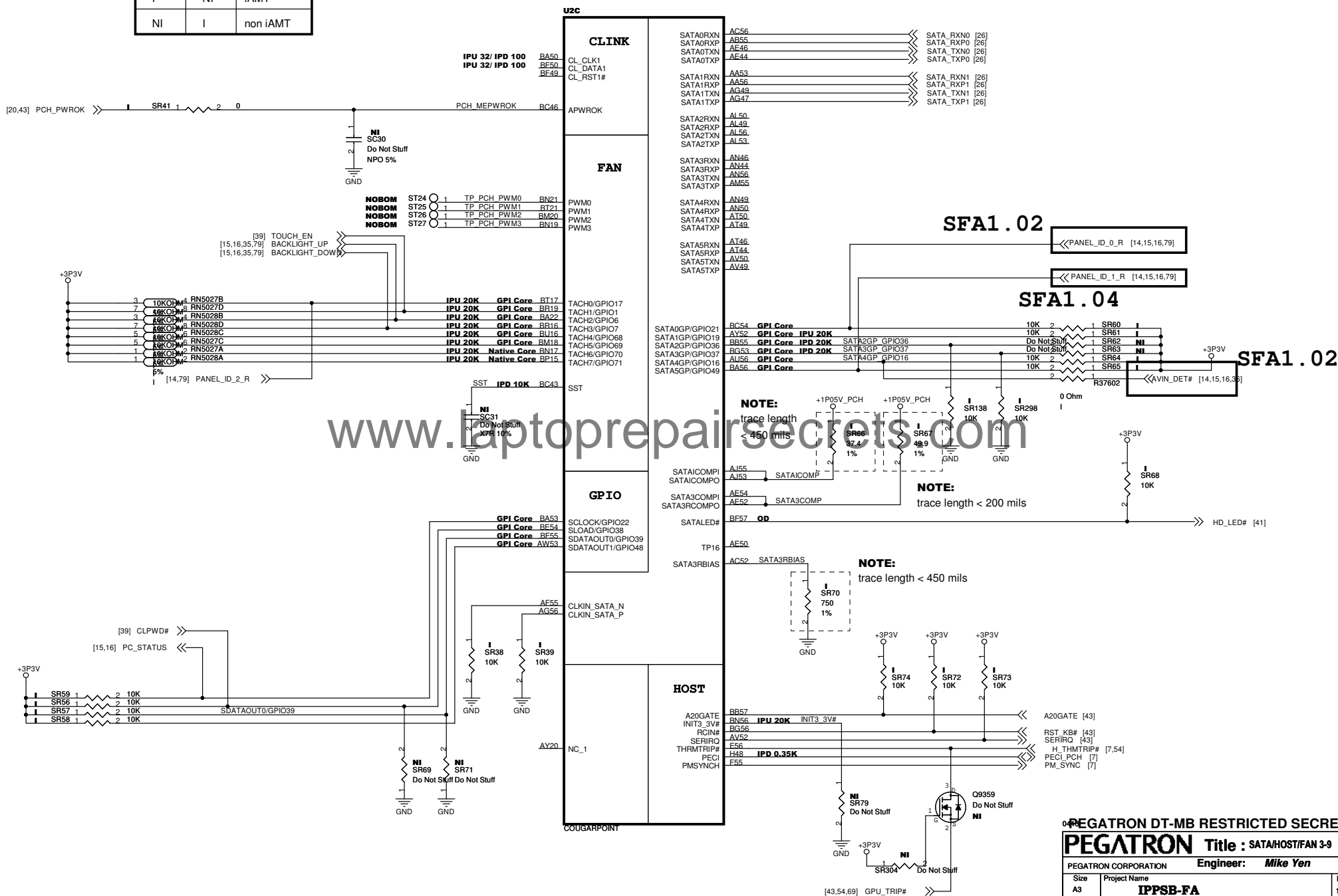
PEGATRON Title : PCIe/USB/DMI 2-9

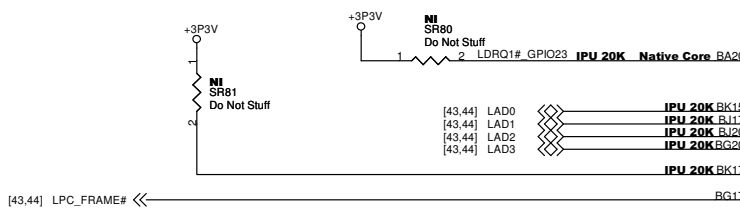
PEGATRON CORPORATION Engineer: Mike Yen

Size A3 Project Name IPPSB-FA Rev 1.01

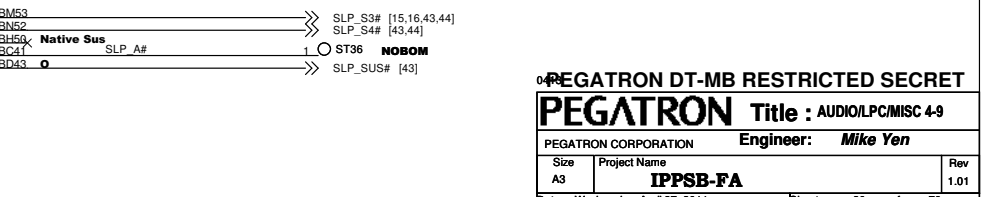
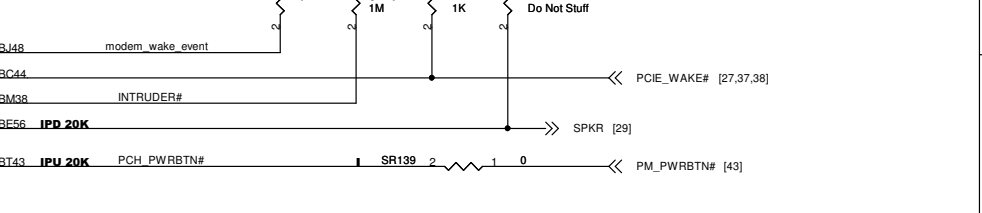
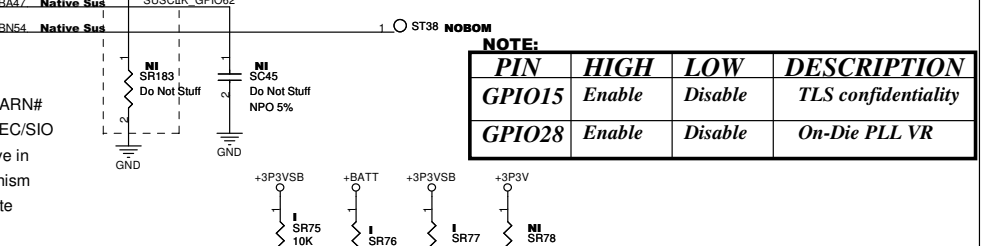
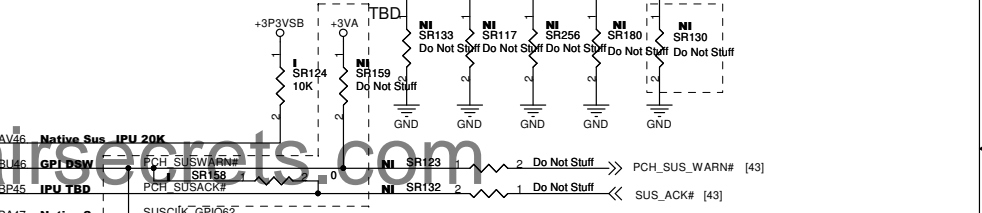
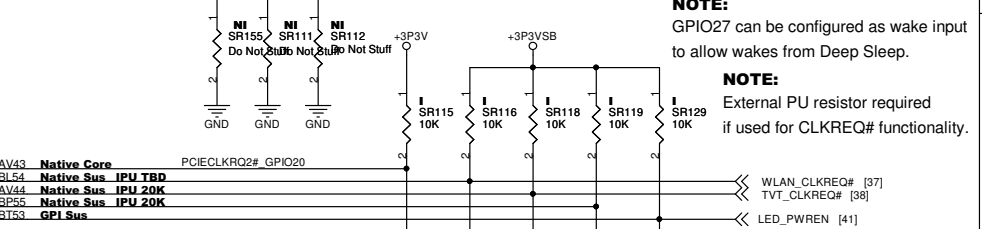
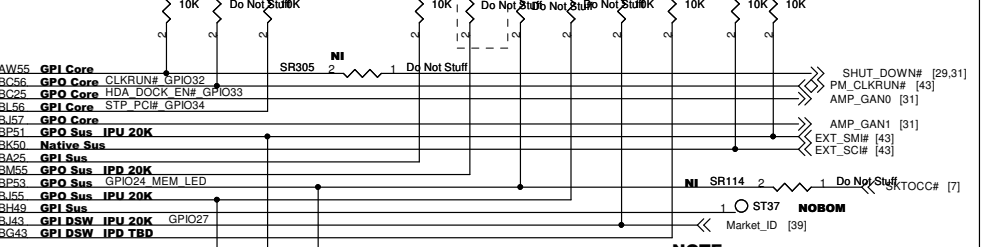
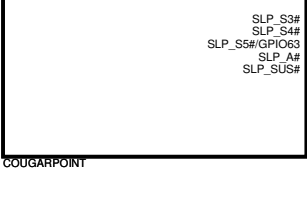
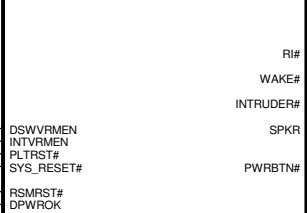
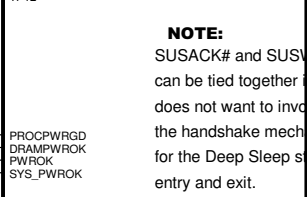
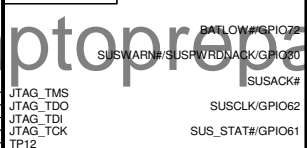
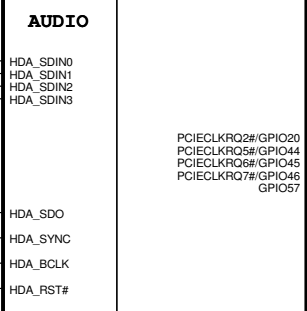
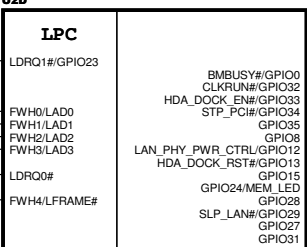
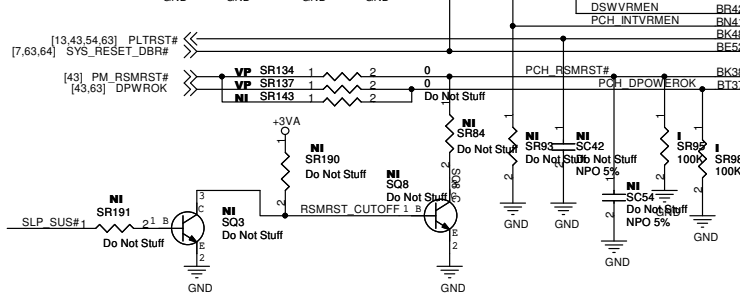
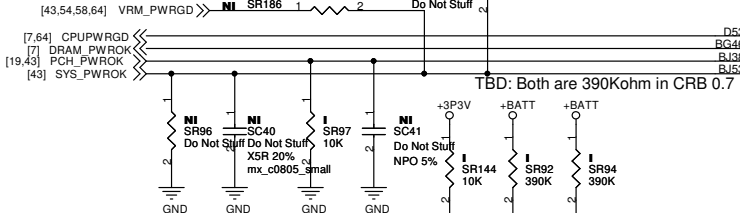
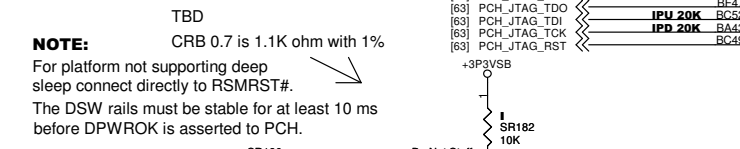
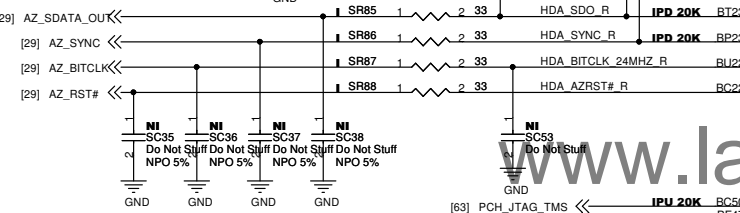
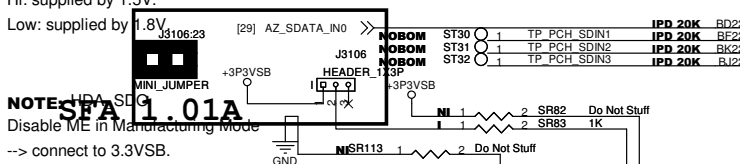
Date: Wednesday, April 27, 2011 Sheet 18 of 79

SR40	SR41	Description
I	NI	iAMT
NI	I	non iAMT

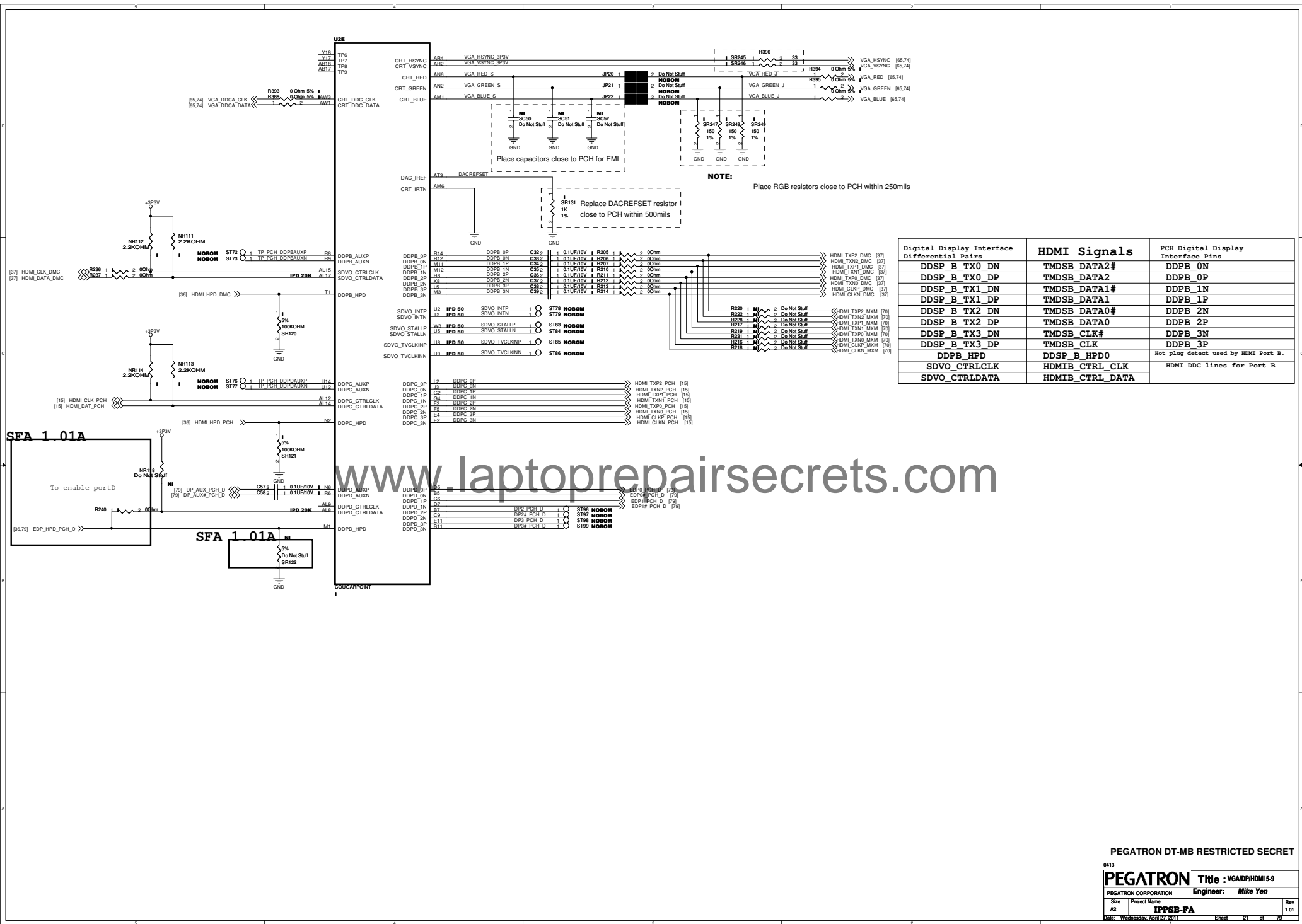




NOTE: HDA_SYNC
On-die PLL VR voltage selector.
Hi: supplied by 1.5V.
Low: supplied by 1.8V.



PIN	HIGH	LOW	DESCRIPTION
GPIO15	Enable	Disable	TLS confidentiality
GPIO28	Enable	Disable	On-Die PLL VR



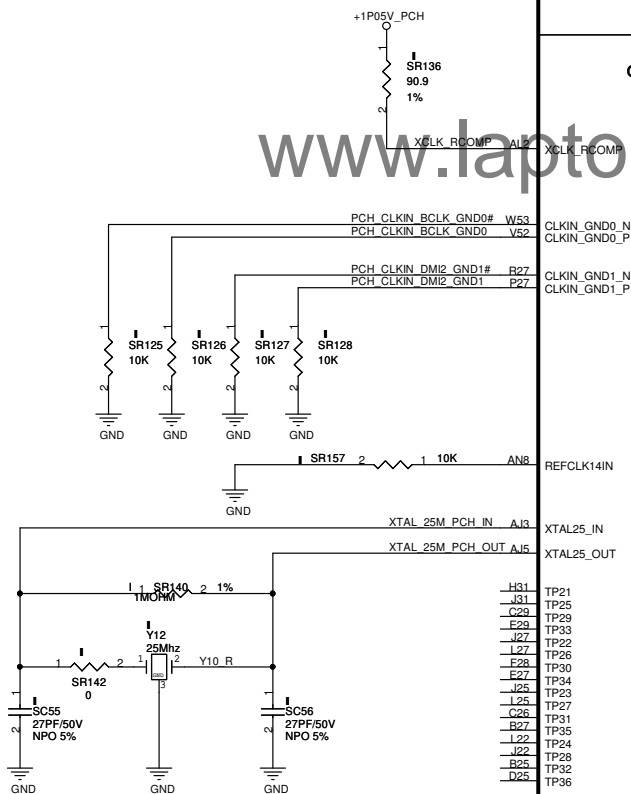
PEGATRON DT-MB RESTRICTED SECRET

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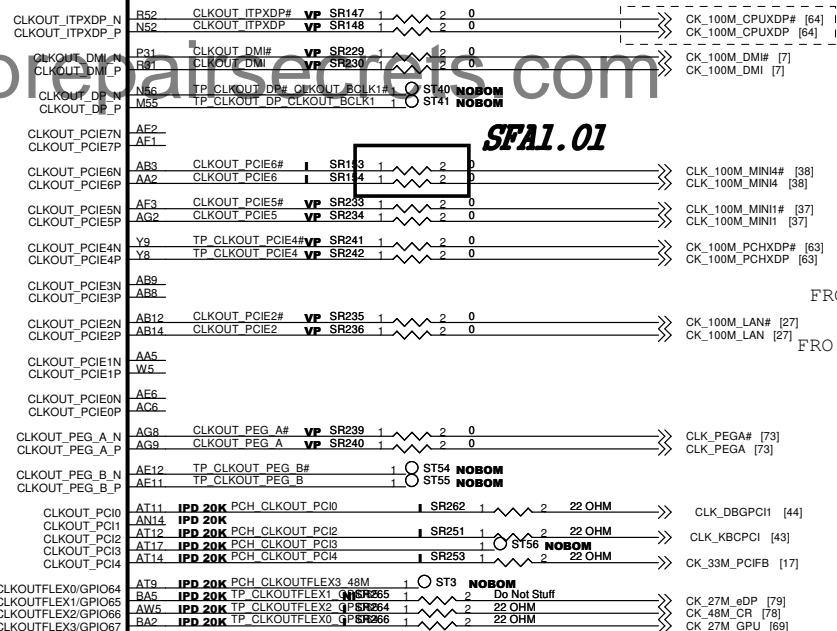
PEGATRON		Title : VGA/DP/HDMI 5-9	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size	Project Name	Rev	
A0	IPPSB-FA	1.01	
Date: Wednesday, April 27, 2011		Sheet	21 of 79

[7] PROC_SEL

Place HR23 close to NVRAM connector
and minimize this stub to <100 mils
with PCH and NVRAM connector



CLOCK



NOTE:

1. Prioritize 27/14/24/48/25-MHz FLEX on FLEX1/3.
2. Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0/2 if more than 2 PCI clocks + PCI loopback are routed.
3. With 2 PCI clocks routed (or less), prioritize the FLEX clocks to FLEX1/3 a. 27MHz(SSC/non-SSC) b. 14.31818MHz c. 24/48 d. 25MHz

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON CORPORATION		Project Name		Rev
Size		IPPSB-FA		1.01
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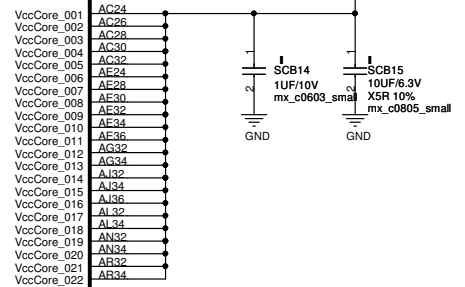
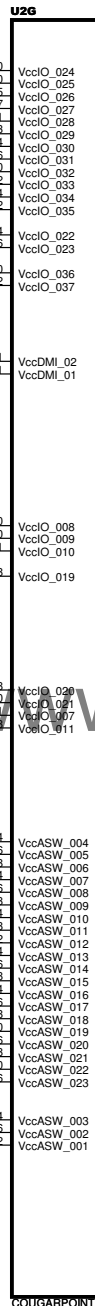
NOTE:
Install those cap during initial power-on.

NOTE:
Splitting 2 power trace/shape
on pin Y20/Y22/V22 to other pins

NOTE:
Trace needs
to be at least
20 mils width
with full VSS/
VCC reference
plane

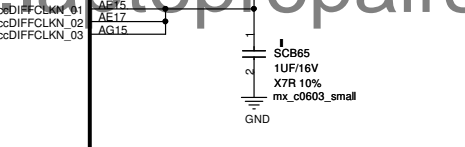
NOTE:
Splitting 2 power trace/shape

NOTE:
Install SCB12 during initial power-on.



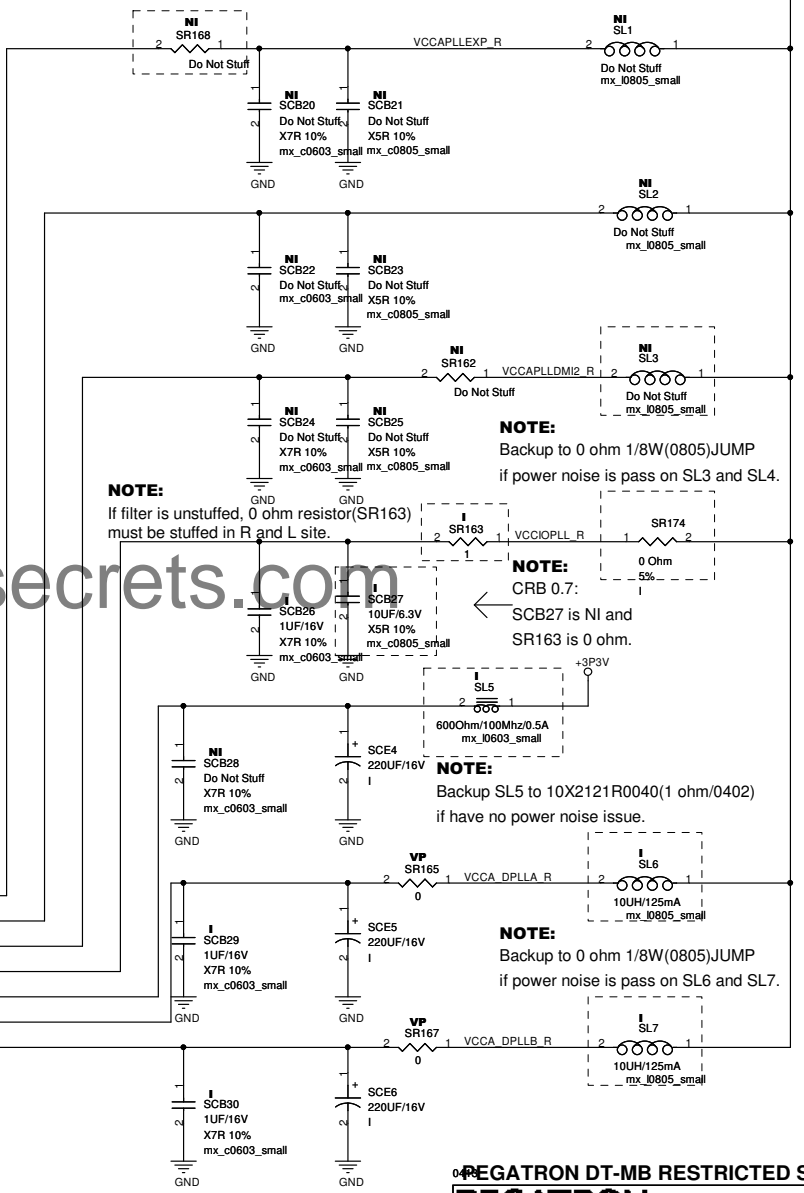
NOTE:
Splitting 2 power trace/shape
on pins AV24/AV26 to AY25/AY27,
and AE40 to AG38/AG40.

NOTE:
Splitting 2 power traces
on pins AC20 to AE20.



NOTE:
VccAFDIPLL and VccACIK
can be NC in on-die VR mode.

NOTE:
VccAPLLEXP, VccAPLLSATA, and VccAPLLDMI2 can be NC
in On-Die VR mode.

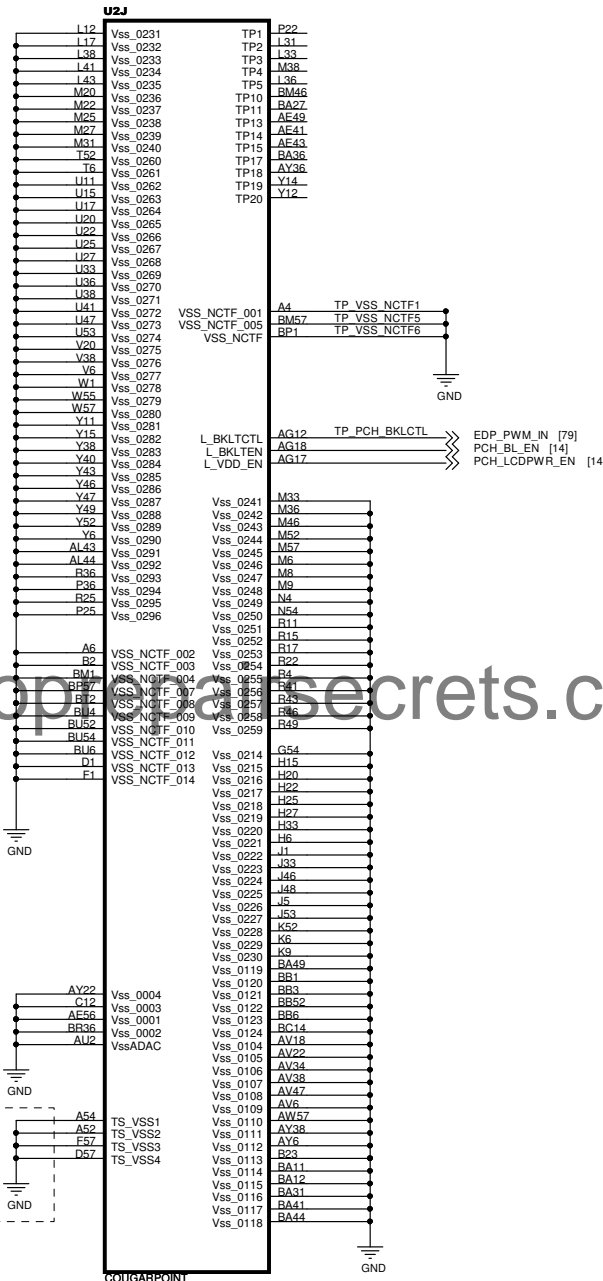
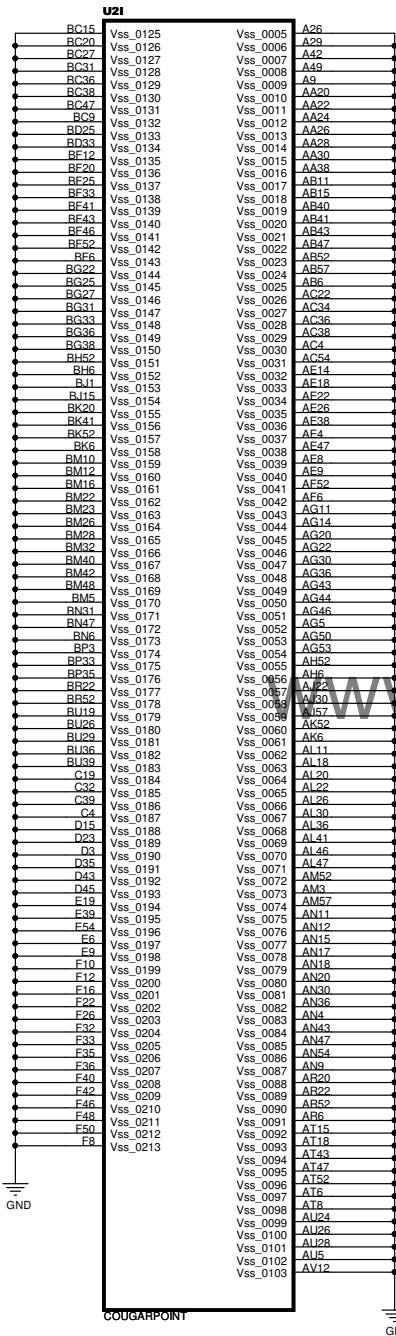


NOTE:
Backup to 0 ohm 1/8W(0805)JUMP
if power noise is pass on SL3 and SL4.

NOTE:
CRB 0.7:
SCB27 is NI and
SR163 is 0 ohm.

NOTE:
Backup SL5 to 10X2121R0040(1 ohm/0402)
if have no power noise issue.

NOTE:
Backup to 0 ohm 1/8W(0805)JUMP
if power noise is pass on SL6 and SL7.

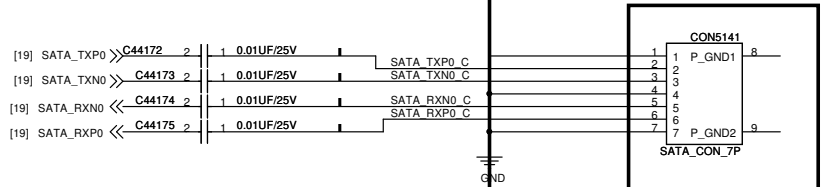


NOTE:
BOM option depend on thermal result

已更改完成

SATA HDD CON

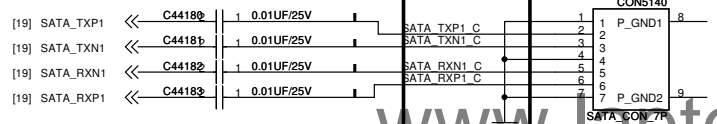
1.01 20101019 revised



**SATA CONTROLLER #1
(MASTER)
COLOR = DARK BLUE**

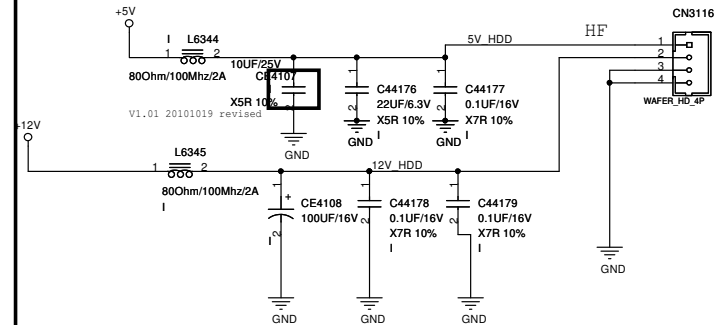
SATA ODD CON

1.01 20101019 revised

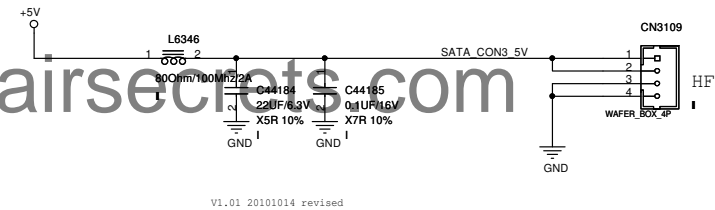


**SATA CONTROLLER #2
(SLAVE)
COLOR = WHITE**

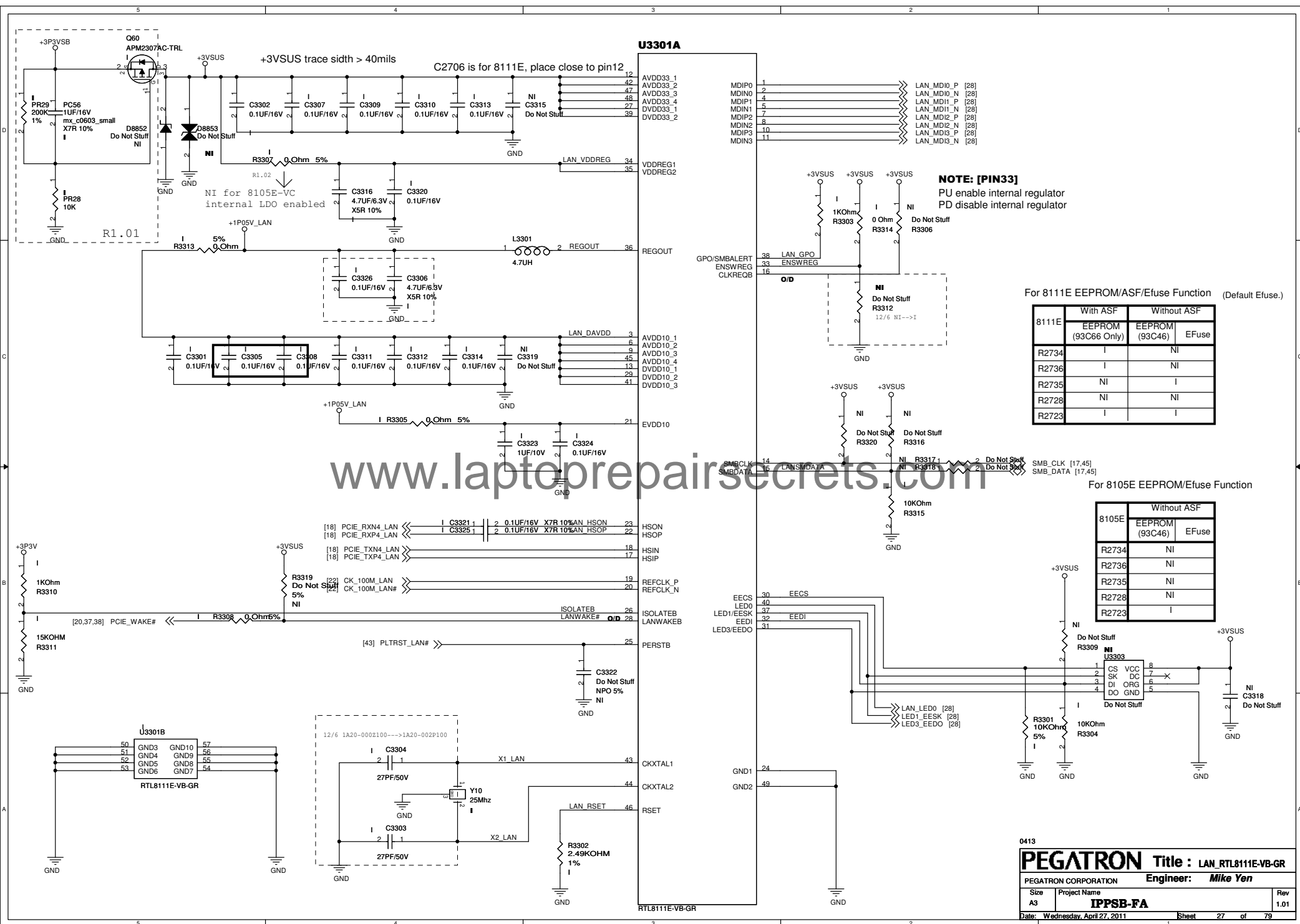
SATA POWER CONN.



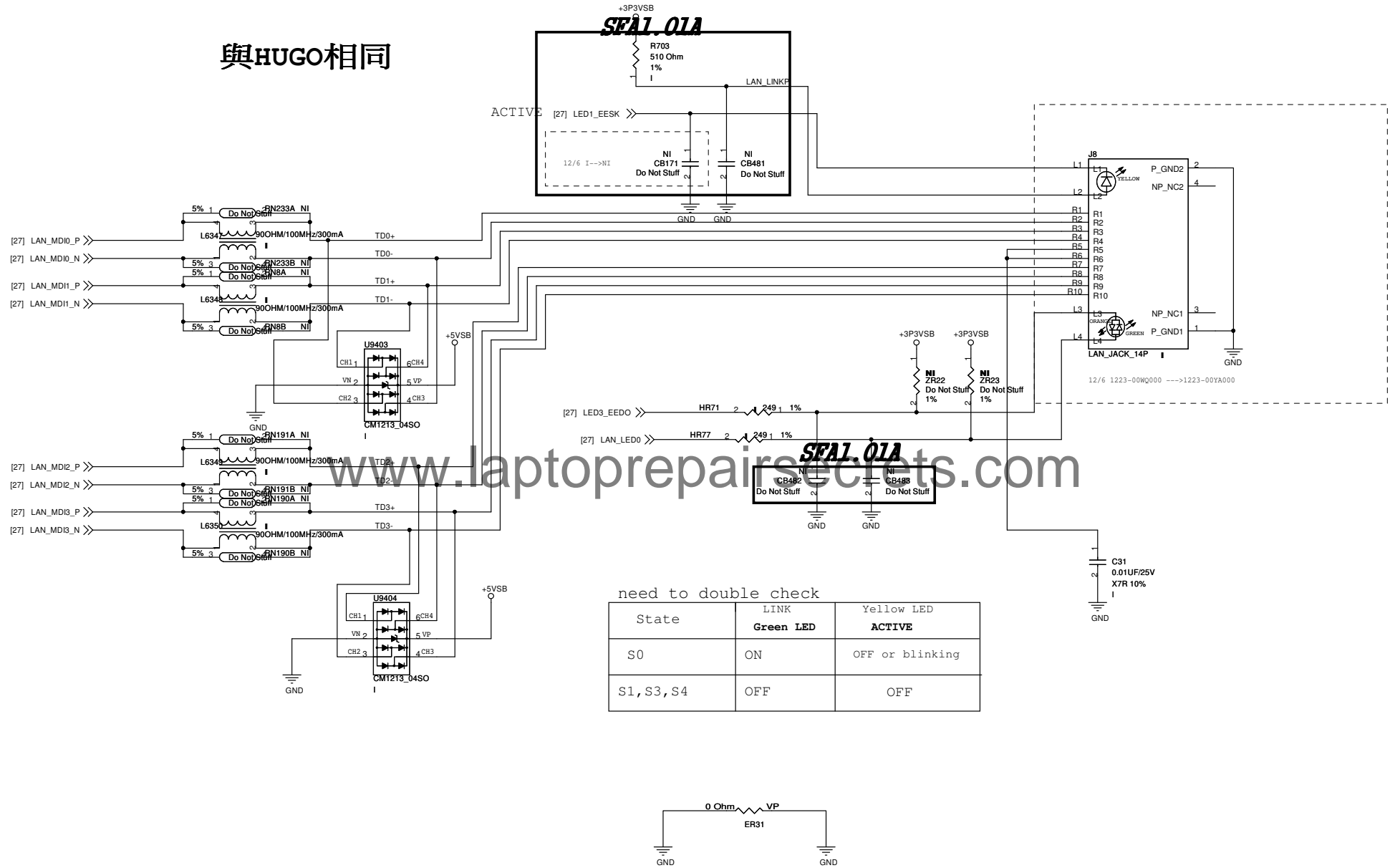
ODD POWER CONN.

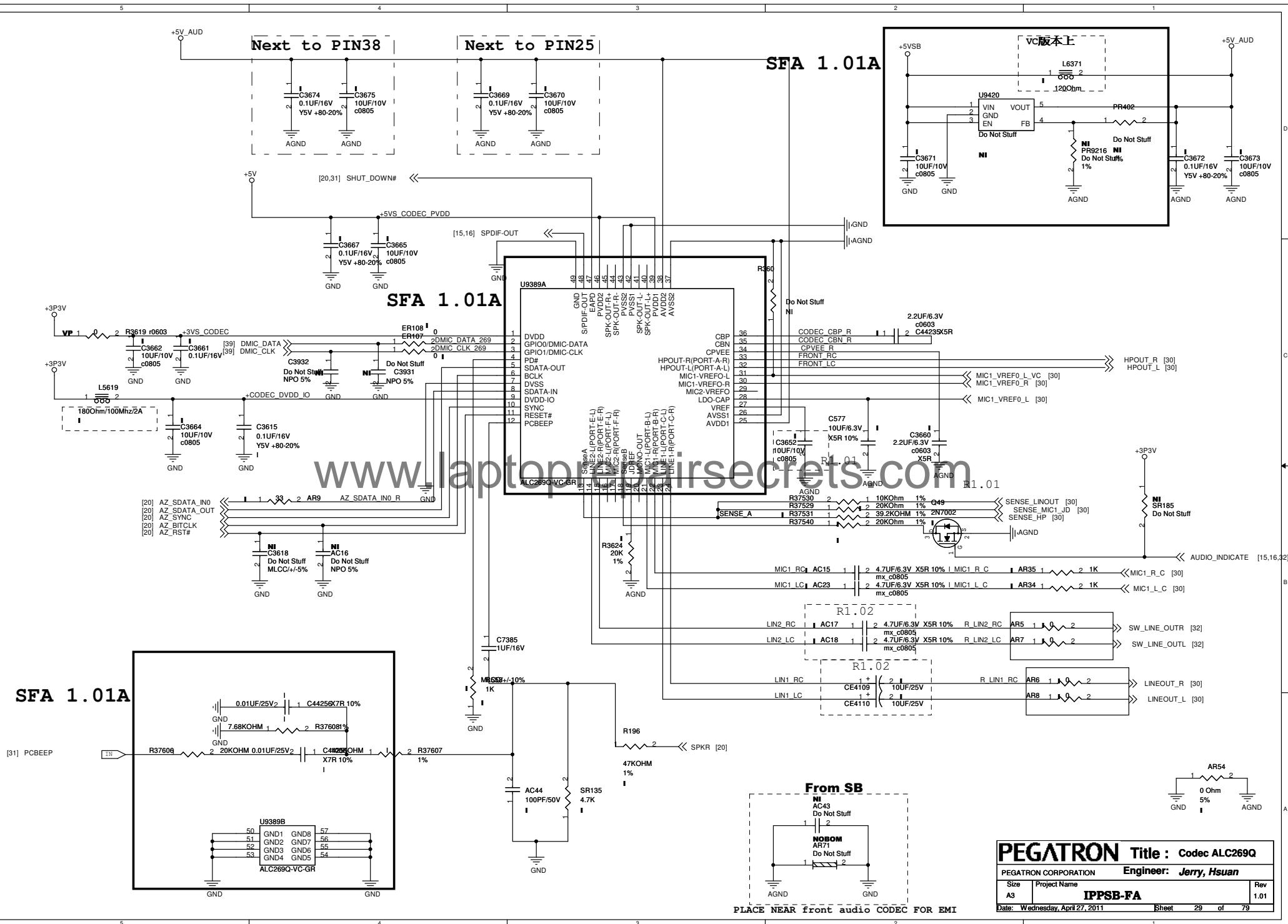


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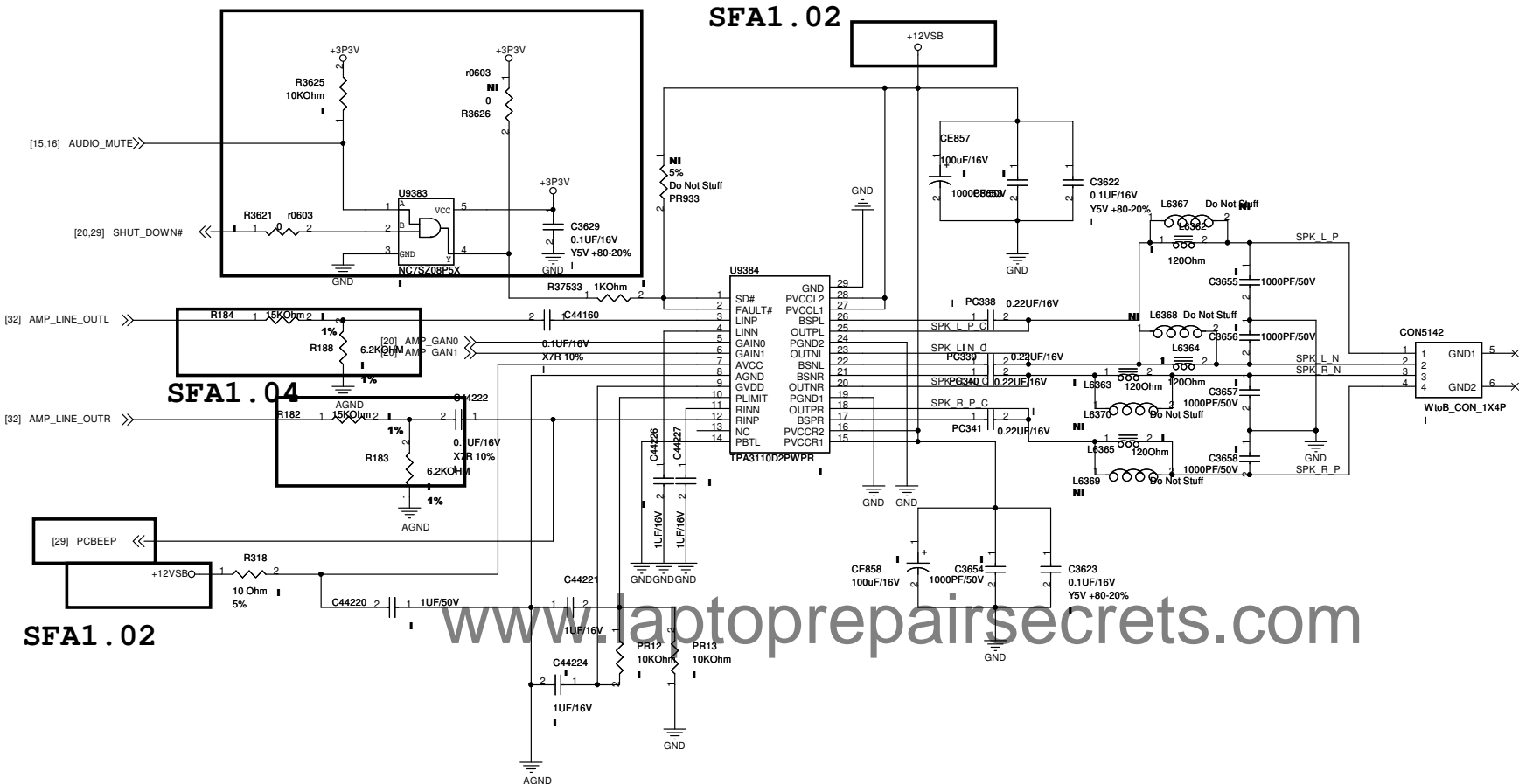
與HUGO相同





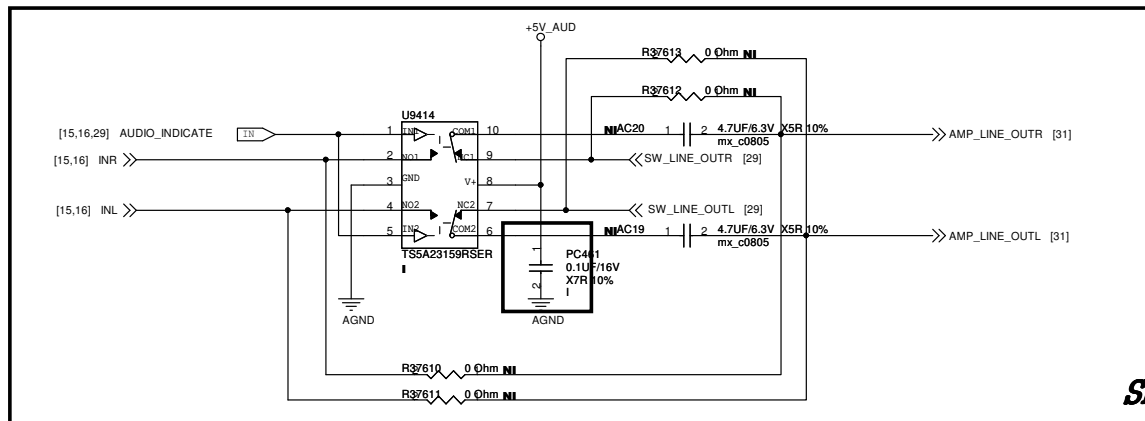


SFA1.02



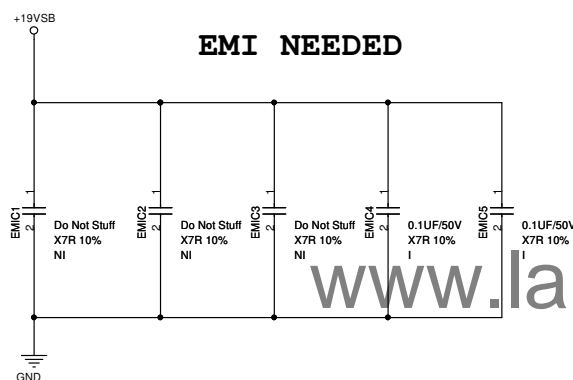
SFA1.02

PEGATRON Title : Amp TPA3100D2			
PEGATRON CORPORATION		Engineer: Jerry, Hsuan	
Size	Project Name		Rev
A3	IPPSB-FA		1.01
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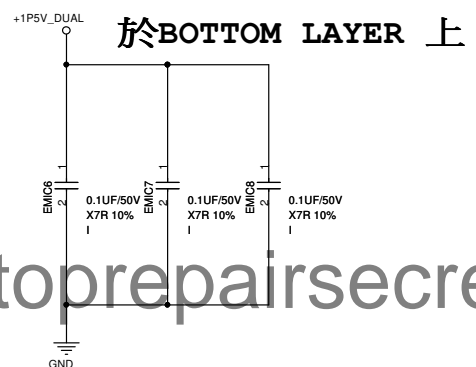


SFA1.04

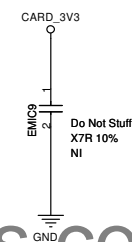
EMI NEEDED



於BOTTOM LAYER 上

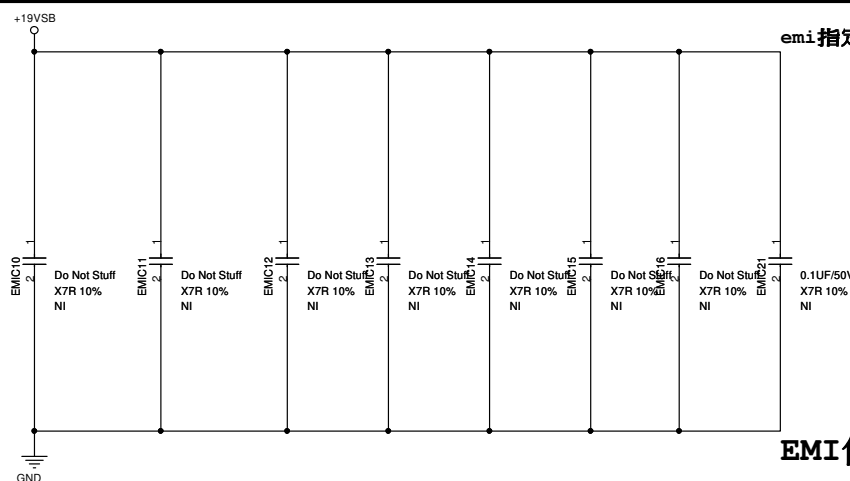


於TOP LAYER 上



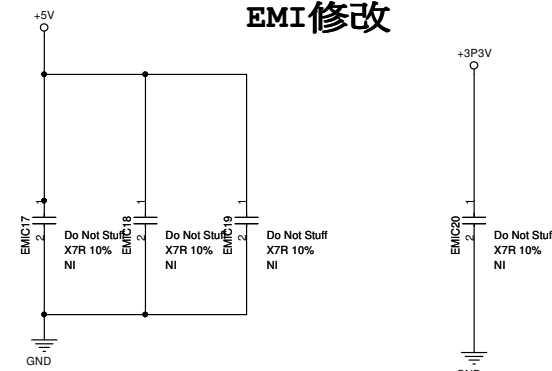
www.laptoprepairsecrets.com

emi指定位置

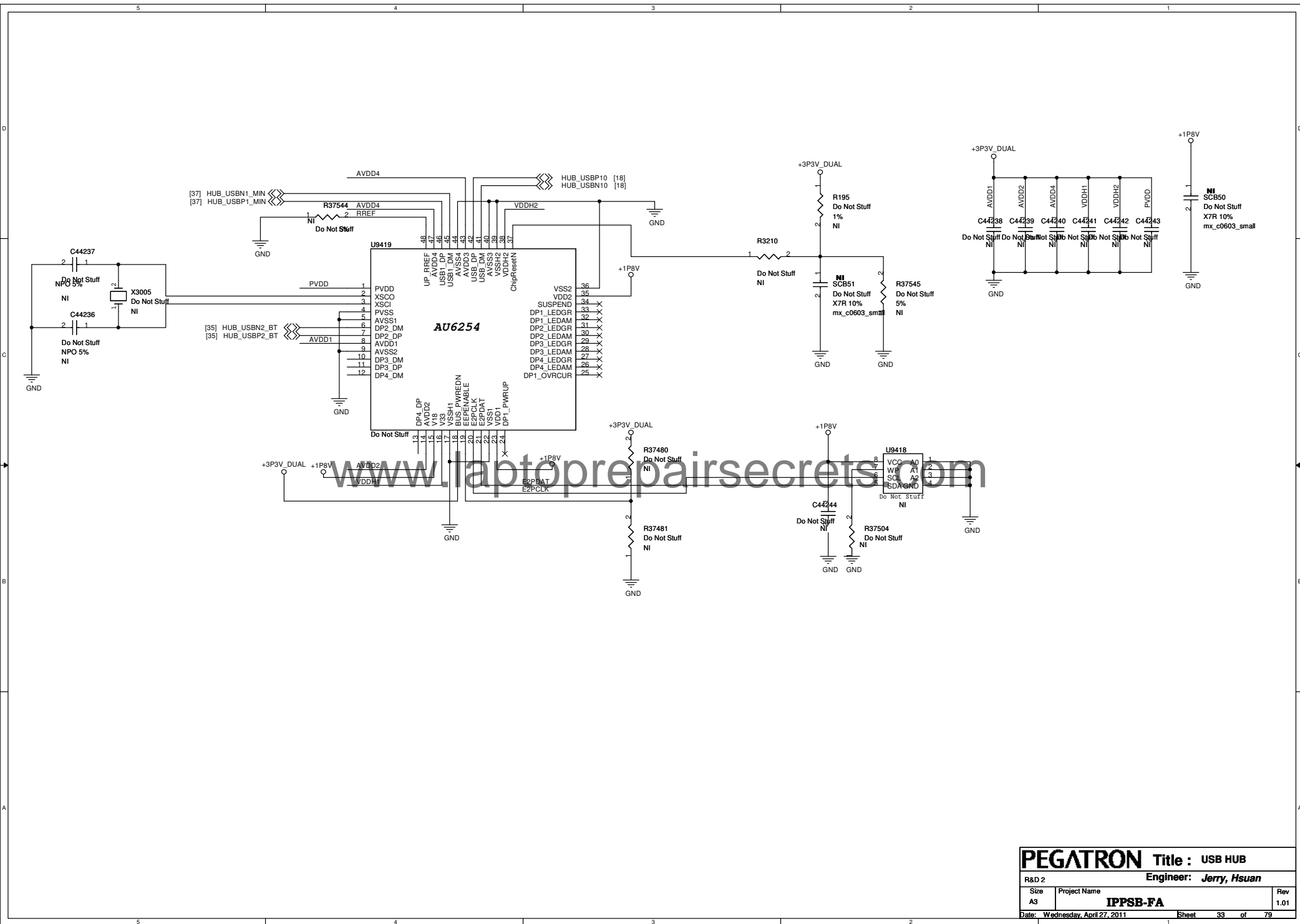


EMI修改

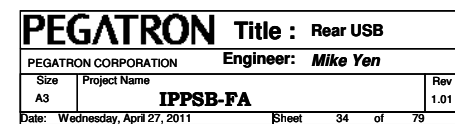
EMI修改



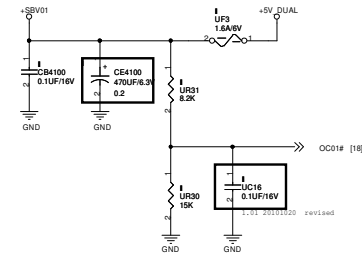
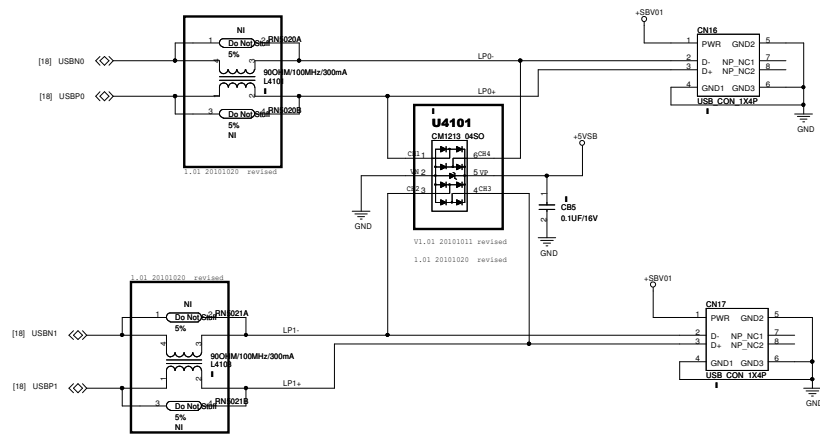
PEGATRON			Title : Amp SW &EMI	
PEGATRON CORPORATION			Engineer: Jerry, Hsuan	
Size A3	Project Name IPPSB-FA			Rev 1.01
Date: Wednesday, April 27, 2011		Sheet 32 of 79		



Rear USB2.0 *4

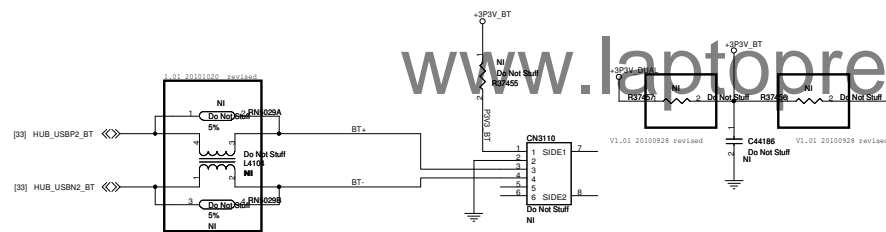


Side USB 已修改過

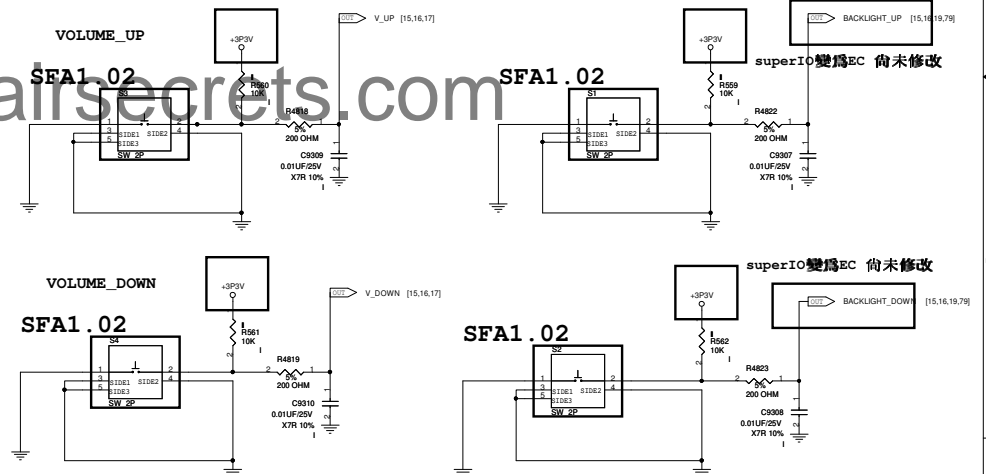


另外增加 Internal I/O BLUE TOOTH

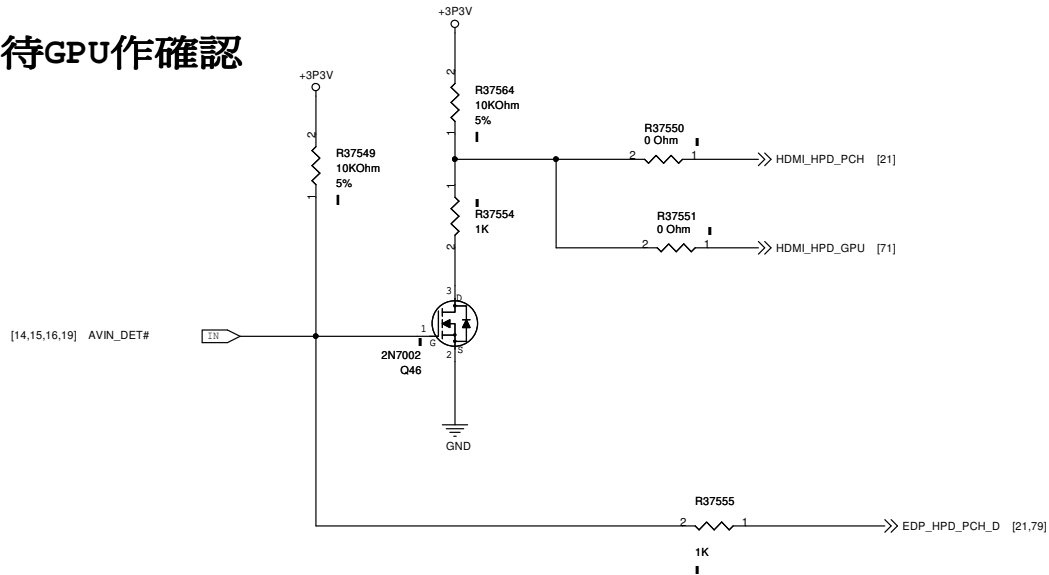
the DMC device connected BT symbols is needed



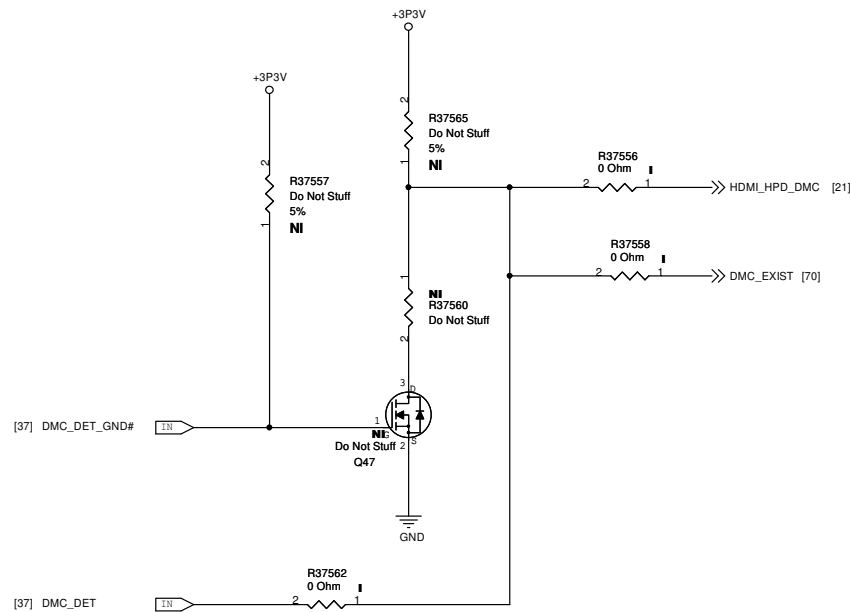
CTRL VOLUME



待GPU作確認



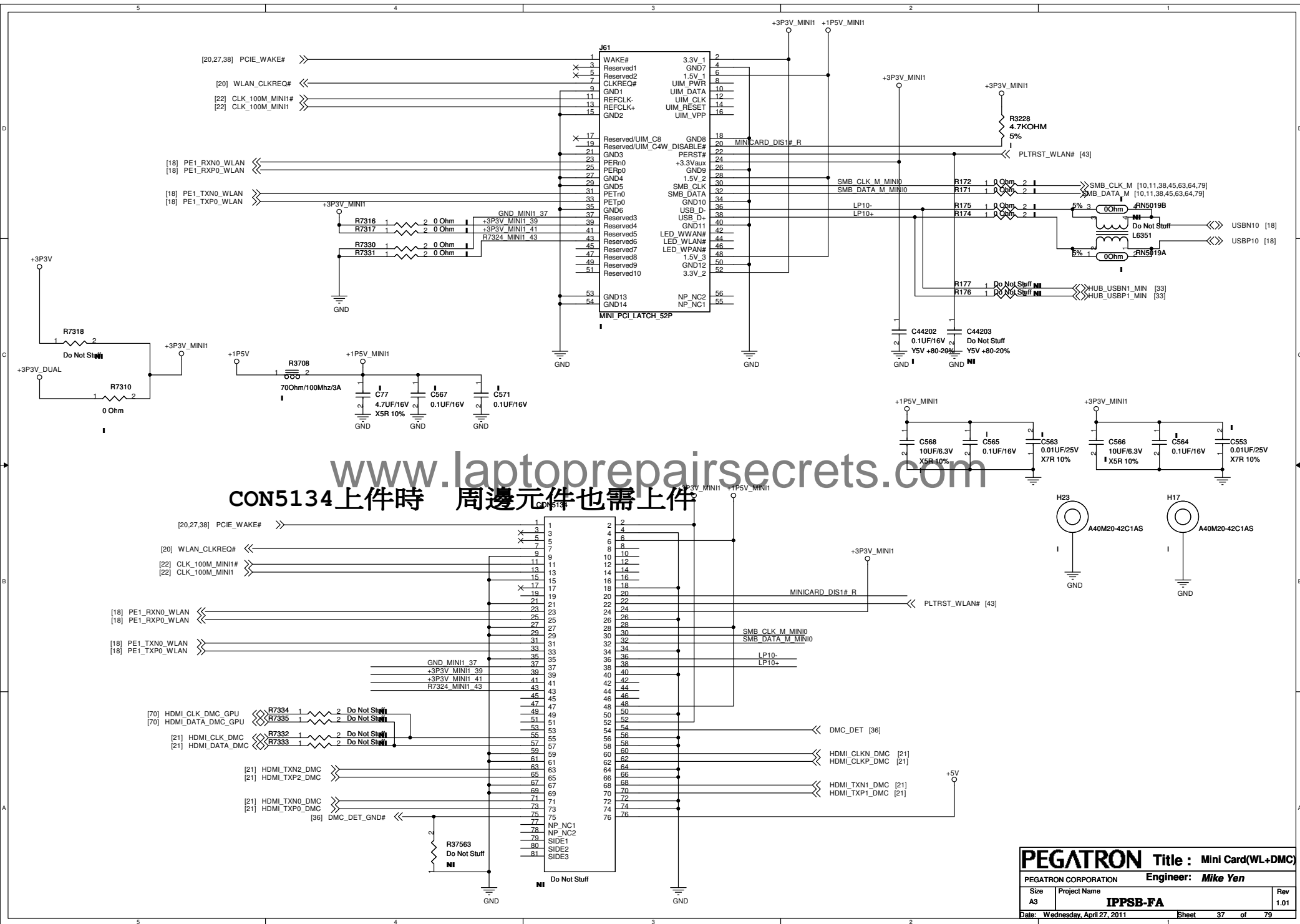
www.laptoprepairsecrets.com

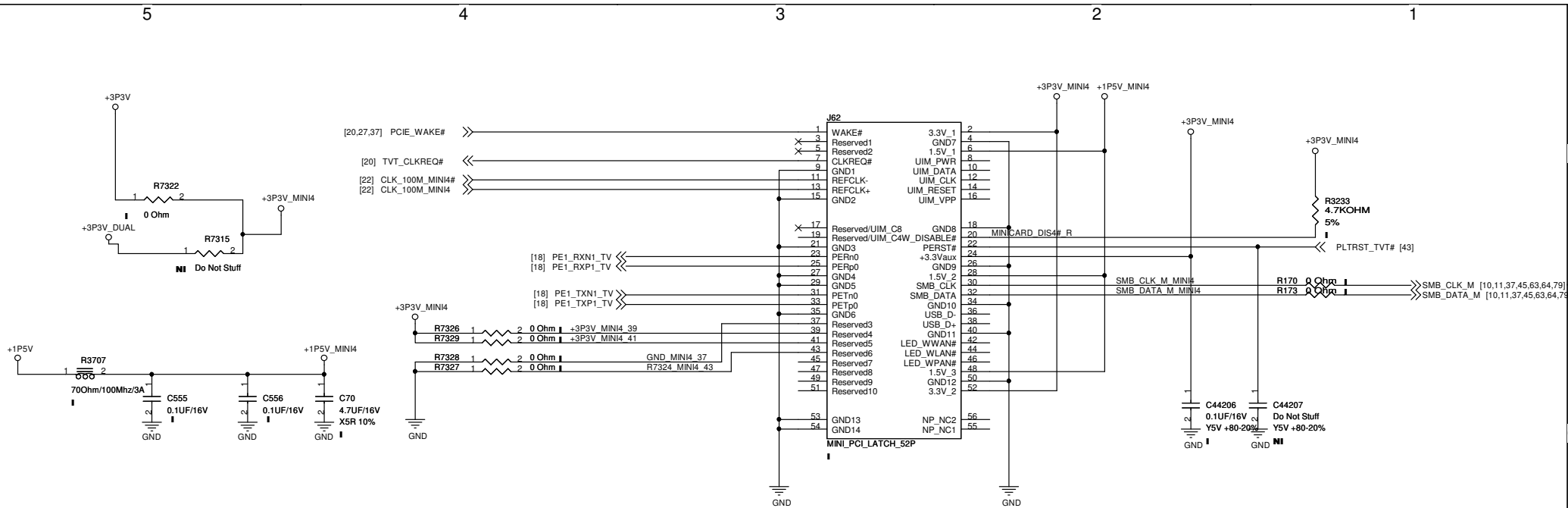


0413

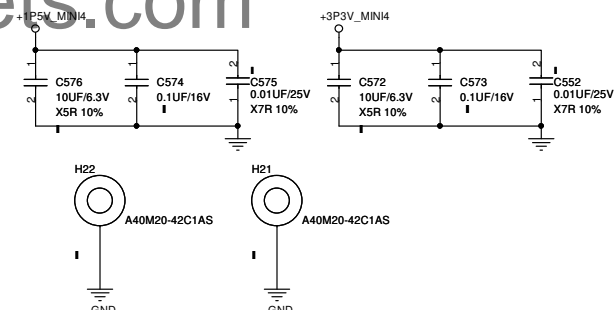
PEGATRON		Title : HPD DET	
R&D 2	Size A3	Project Name IPPSB-FA	Rev 1.01
Date: Wednesday, April 27, 2011		Sheet 36	of 79

Engineer: Jerry, Hsuan



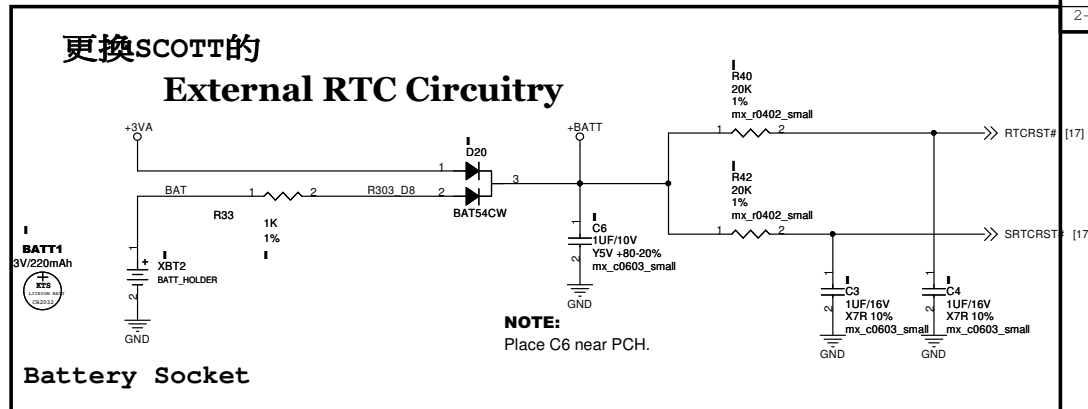


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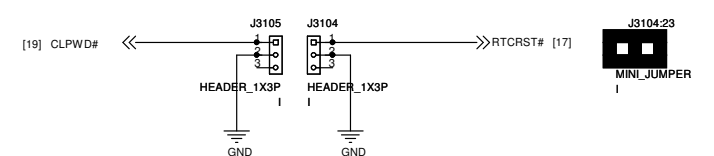


CLR CMOS CIRCUIT

CLR PASSWORD CIRCUIT

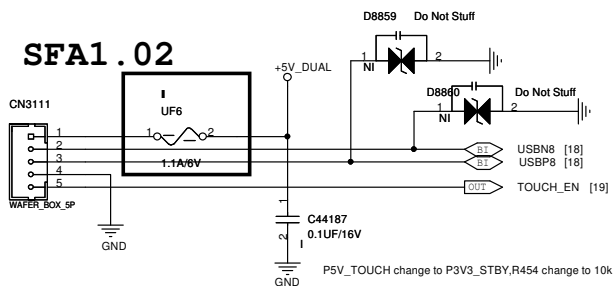


	PASSWORD
1-2	CLEAR
2-3	Default

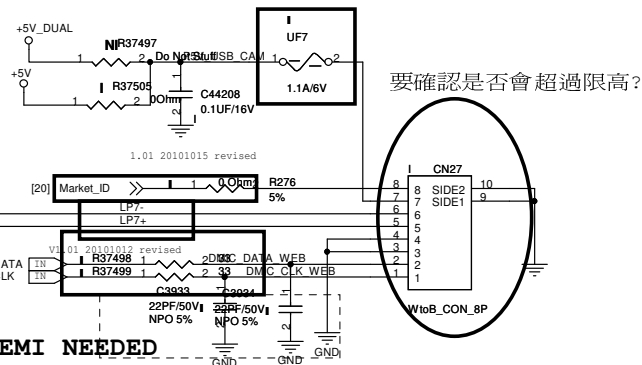


	CMOS RTC
1-2	CLEAR
2-3	Default

TOUCH

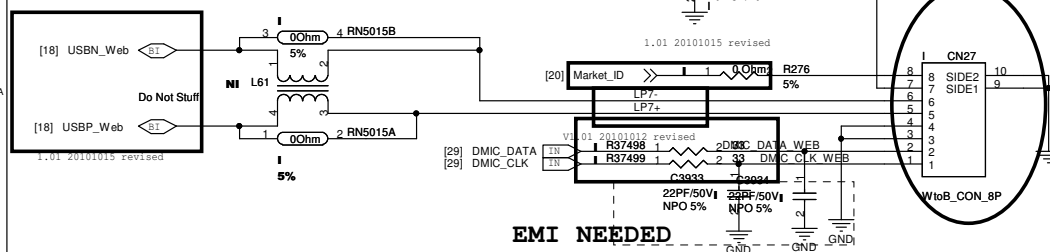


SFA1.03



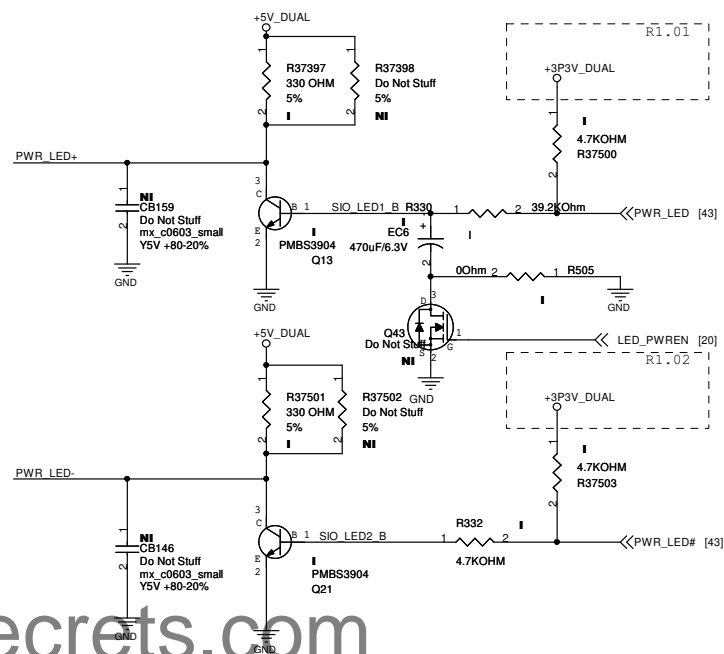
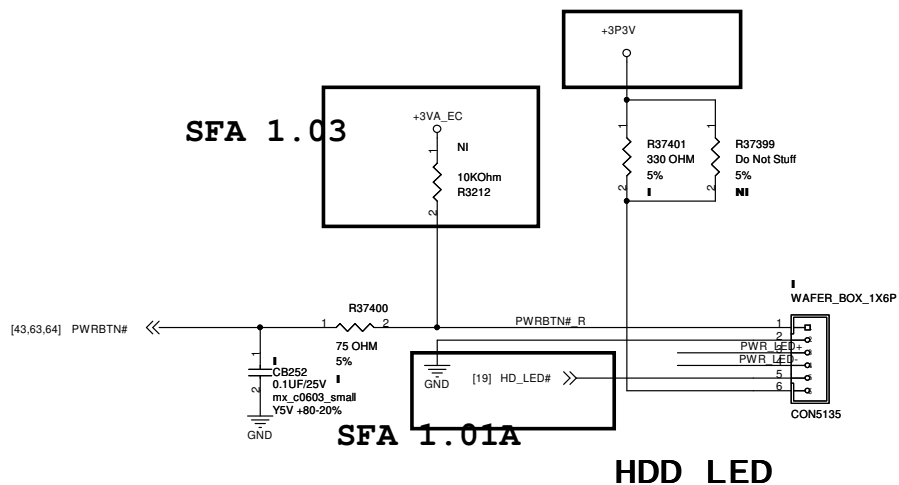
已修改過

AMERA MODULE



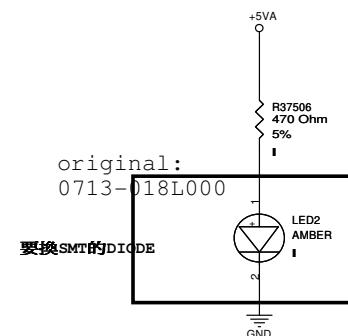
EMI NEEDED

PEGATRON		Title : RTC&CAM&TOUCH	
PEGATRON CORPORATION		Engineer: <i>Mike Yen</i>	
Size A3	Project Name IPPSB-FA	Rev 1.01	
Date: Wednesday, April 27, 2011		Sheet 39 of 79	



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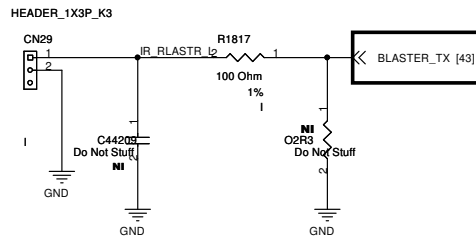
Power supply LED



0413

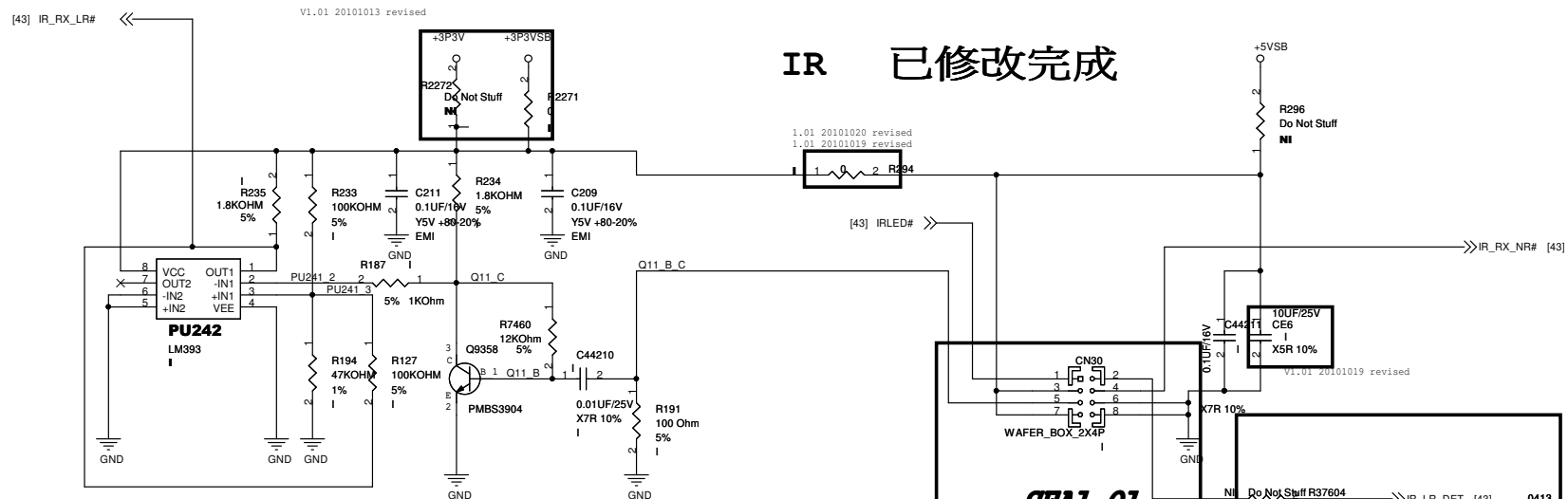
PEGATRON		Title : PWE LED	
PEGATRON CORP.		Engineer: Mike Yen	
Size A3	Project Name IPPSB-FA		Rev 1.01
Date: Wednesday, April 27, 2011		Sheet 41 of 79	

線條未改 IR Blaster



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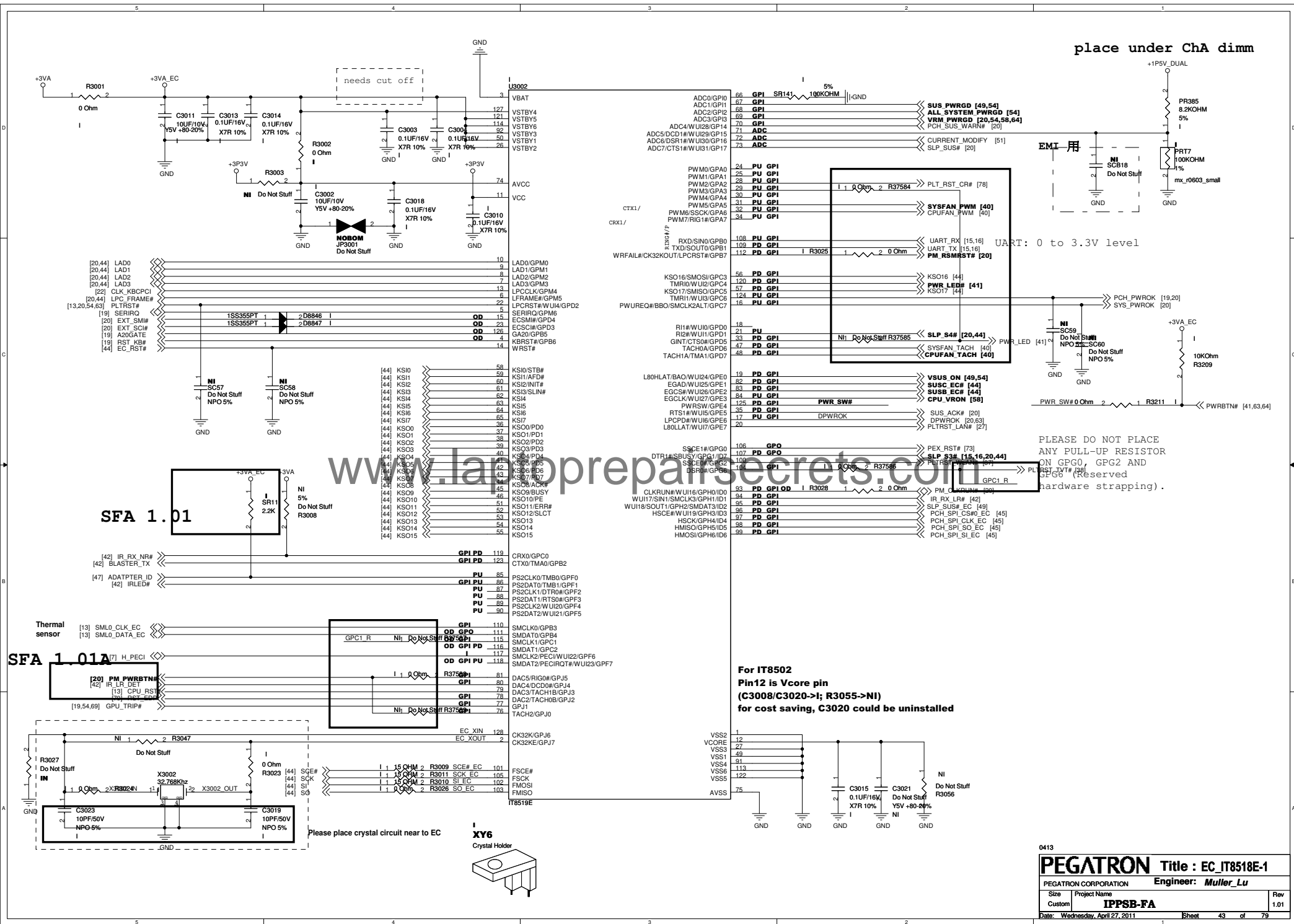
IR 已修改完成



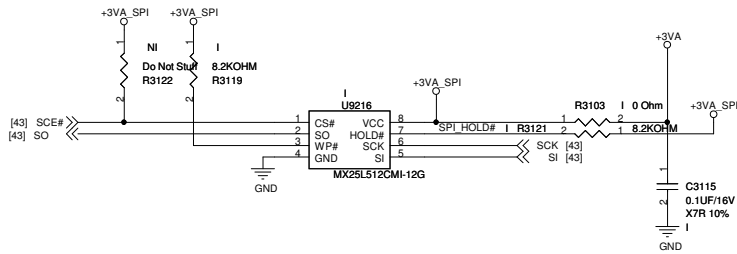
SFA1.01

SFA1.01A

PEGATRON Title : IR LEDs		
PEGATRON CORPORATION		Engineer: Mike Yen
Size A3	Project Name IPPSB-FA	Rev 1.01
Date: Wednesday, April 27, 2011	Sheet 42	of 79



SPI ROM+ External programming conn.

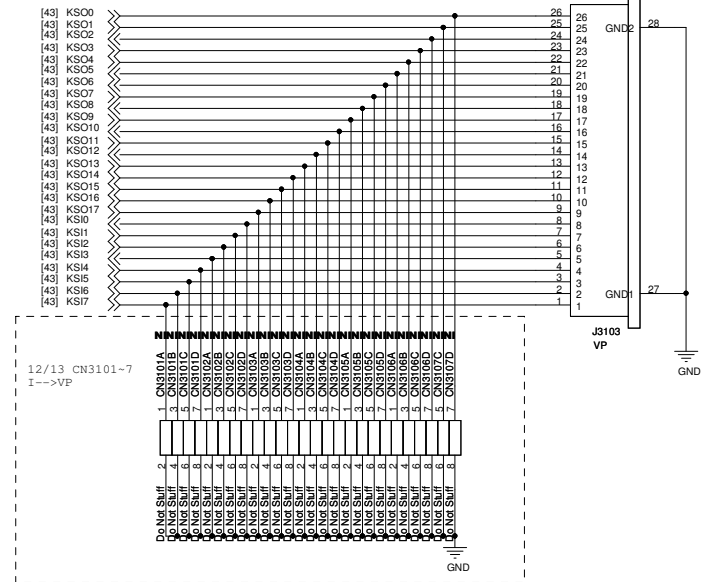


Touch PAD(deleted)

For Instant Key & Switch

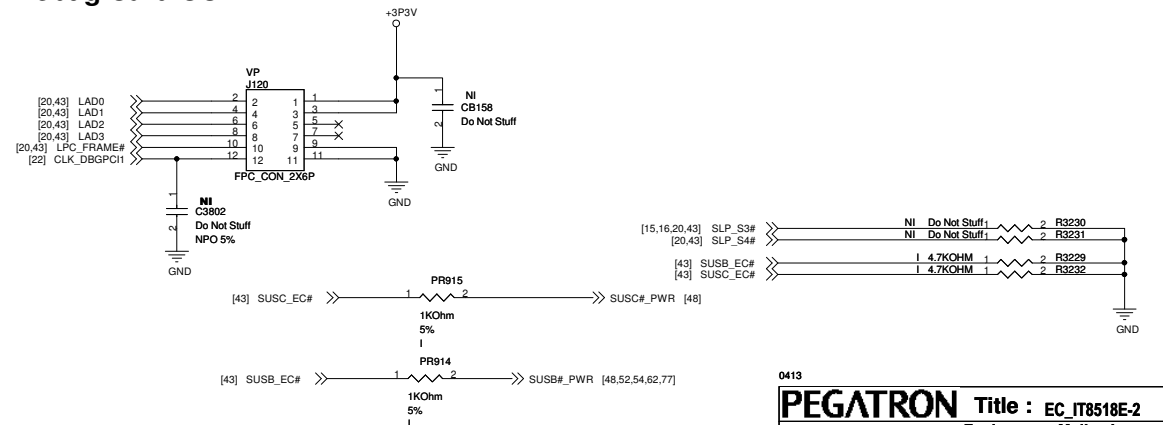
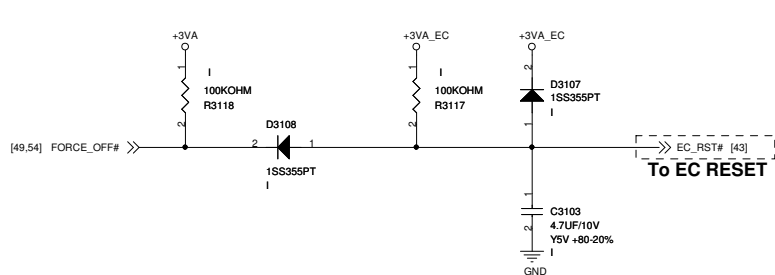
Note: Close to EC

Keyboard Connector(debug)



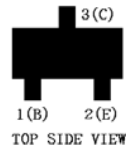
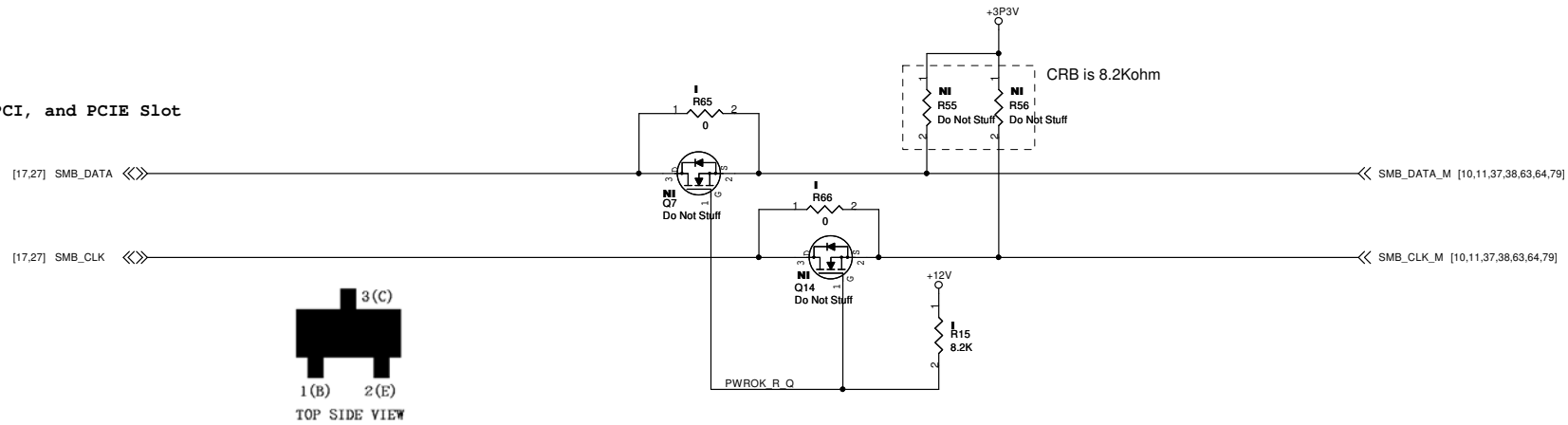
www.laptoprepairsecrets.com For EC PU/PD

Debug Card CON



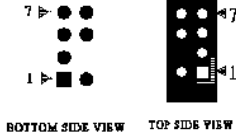
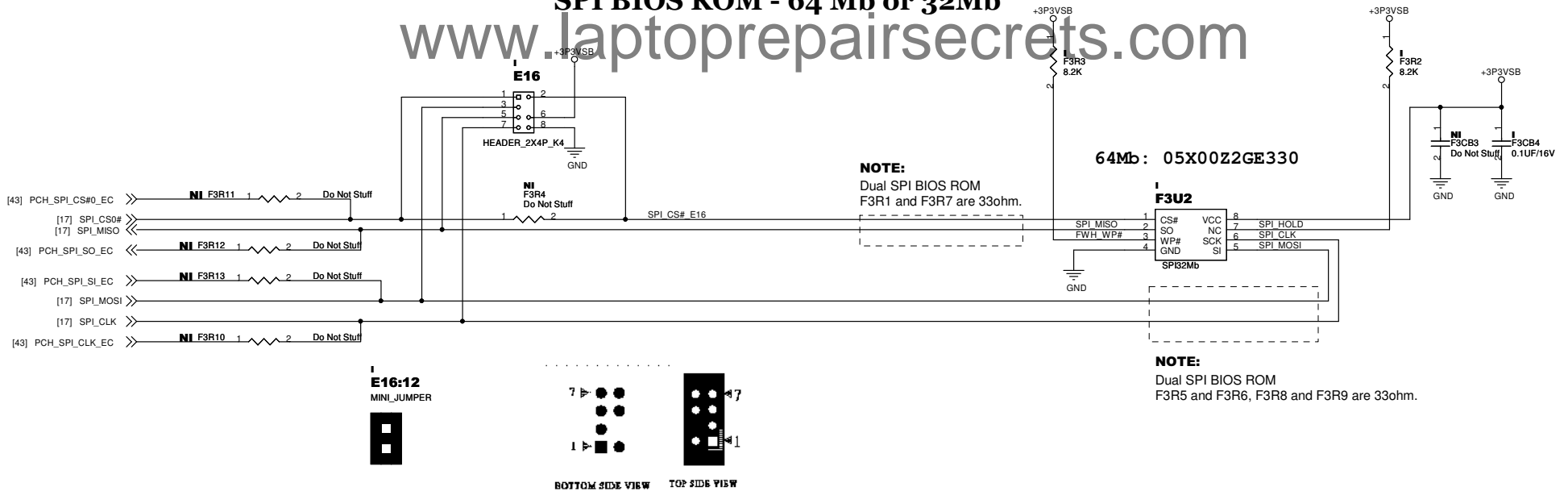
SM BUS Control

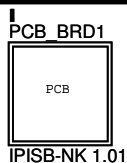
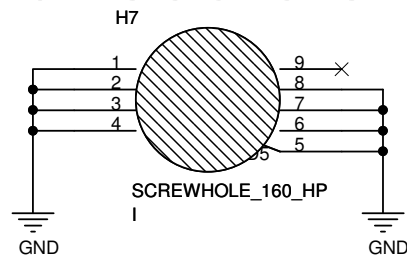
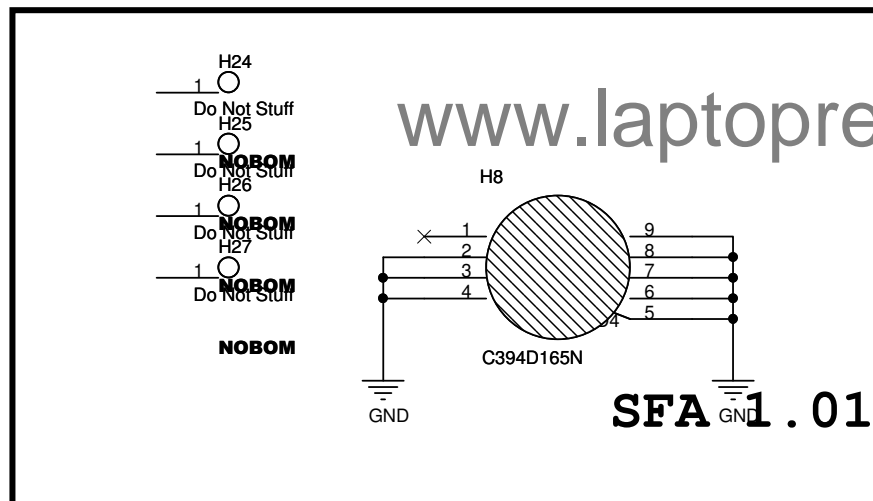
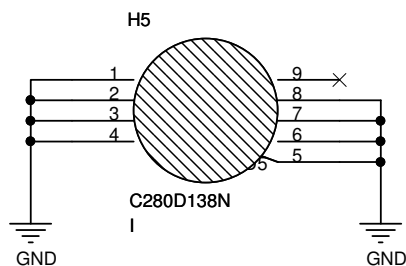
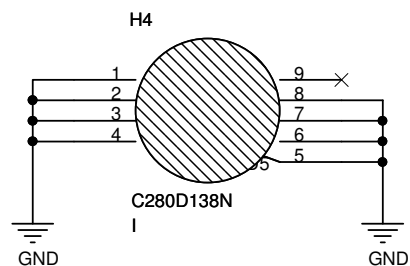
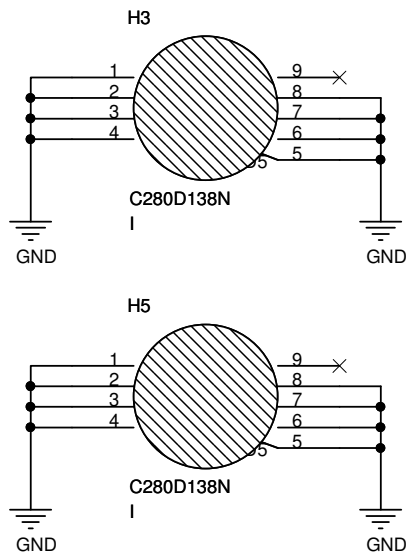
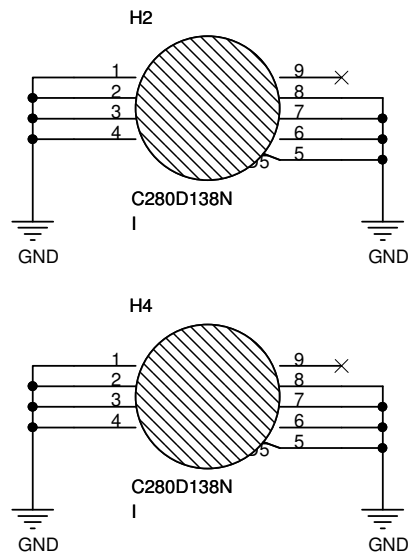
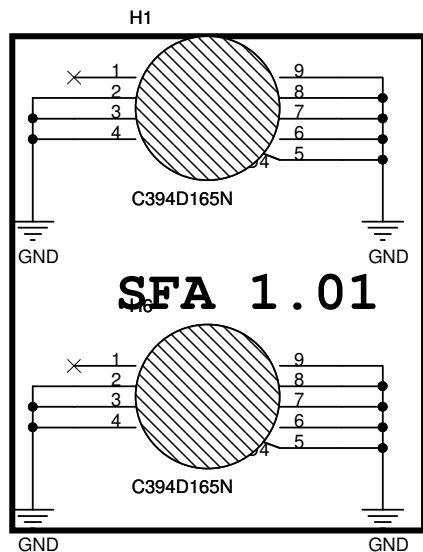
To PCH, PCI, and PCIE Slot



SPI BIOS ROM - 64 Mb or 32Mb

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VESA mount hole

0413

PEGATRON		Title : SCREW HOLE	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size A	Project Name IPPSB-FA		Rev 1.01
Date: Wednesday, April 27, 2011		Sheet	46 of 79

change to SIMULA /AJ261B-Y090-42F, p/n applying....

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PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : UVP, OVP & +19VSB
 PEGATRON CORPORATION Engineer: Mike Yen
 Size Project Name Rev
 A3 IPPSB-FA 1.01
 Date: Wednesday, April 27, 2011 Sheet 47 of 79

change to SIMULA /AJ261B-Y090-42F, p/n applying....

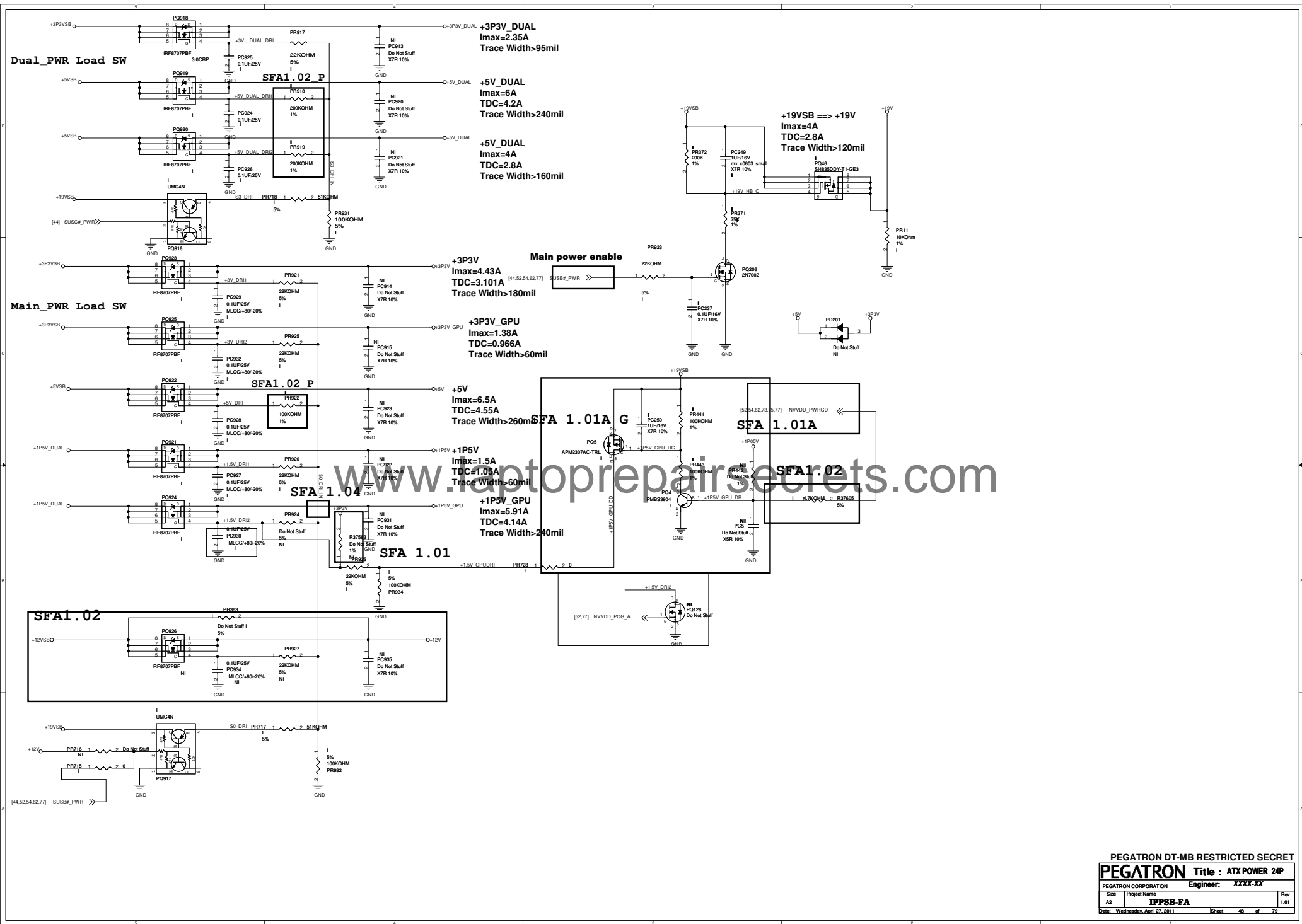
www.laptoprepairsecrets.com

PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : UVP, OVP & +19VSB
 PEGATRON CORPORATION Engineer: Mike Yen
 Size Project Name Rev
 A3 IPPSB-FA 1.01
 Date: Wednesday, April 27, 2011 Sheet 47 of 79

change to SIMULA /AJ261B-Y090-42F, p/n applying....

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PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : UVP, OVP & +19VSB
 PEGATRON CORPORATION Engineer: Mike Yen
 Size Project Name Rev
 A3 IPPSB-FA 1.01
 Date: Wednesday, April 27, 2011 Sheet 47 of 79



PEGATRON DT-MB RESTRICTED SECRET

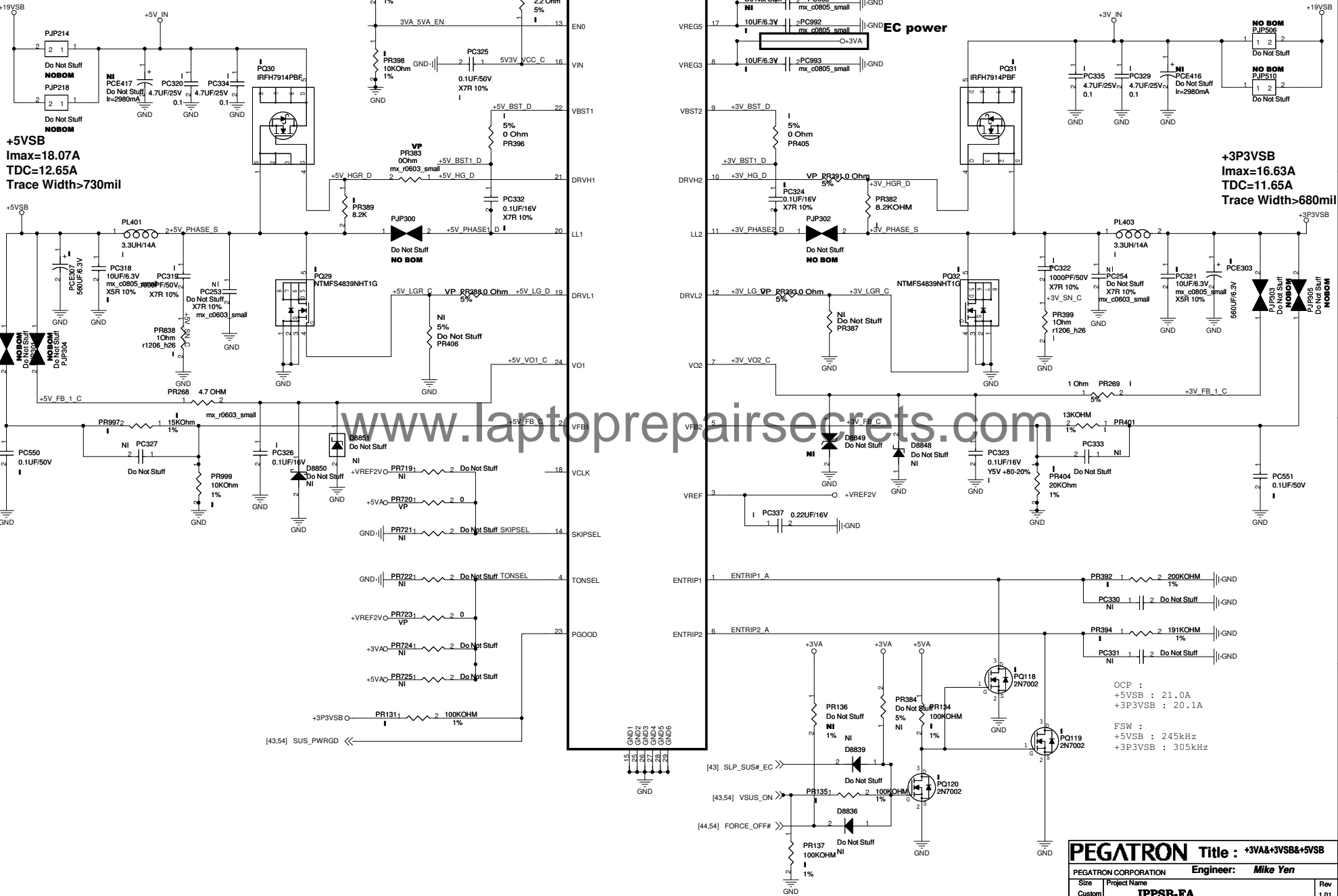
PEGATRON Corporation			
Size		Project Name	
A2		ATX POWER 24P	
Date: Wednesday, April 27, 2011		Sheet 48 of 79	

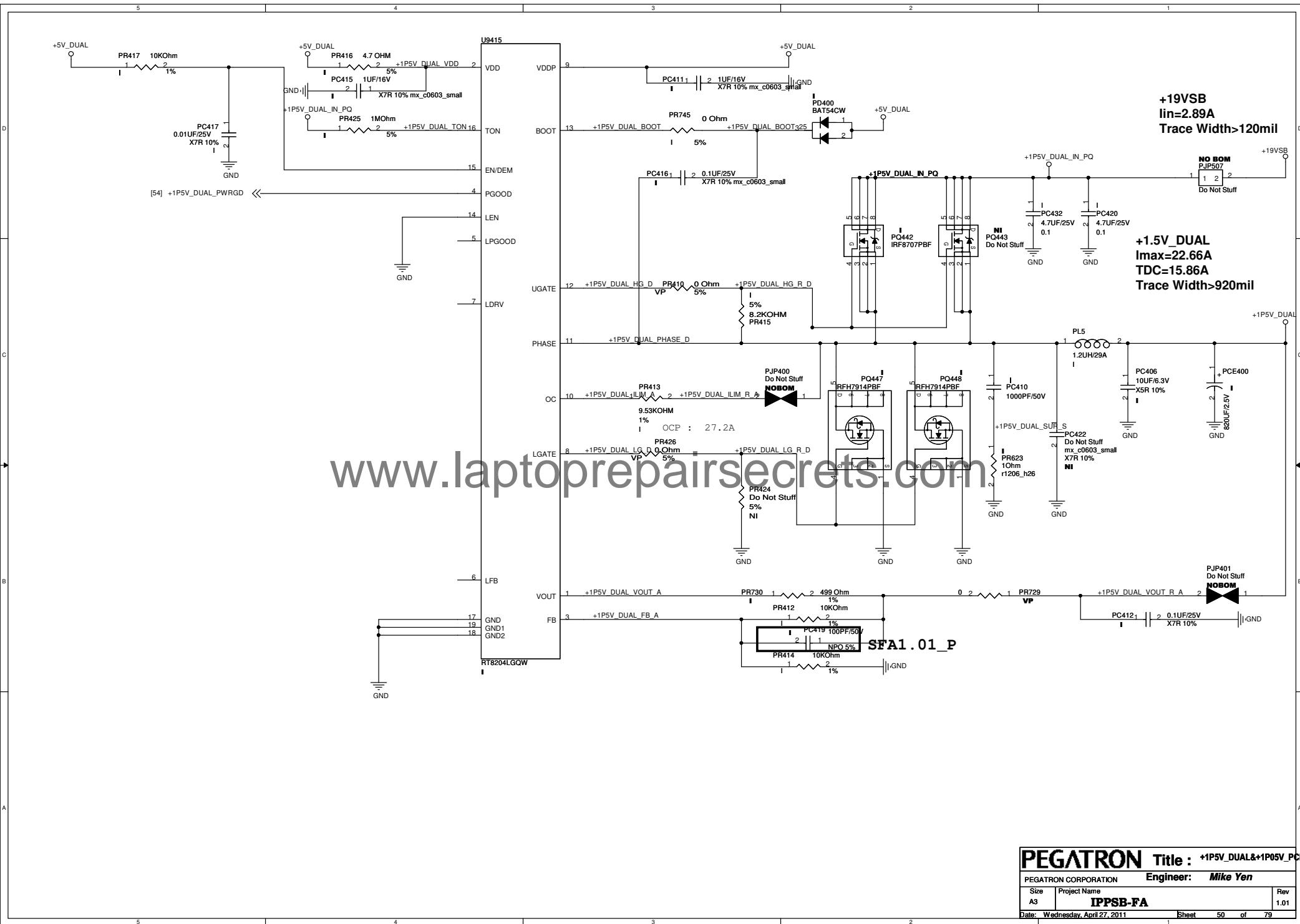
+19VSB
 $I_{in}=5.95A$
 Trace Width>240mil

+5VSB
 $I_{max}=18.07A$
 $TDC=12.65A$
 Trace Width>730mil

+19VSB
 $I_{in}=3.25A$
 Trace Width>130mil

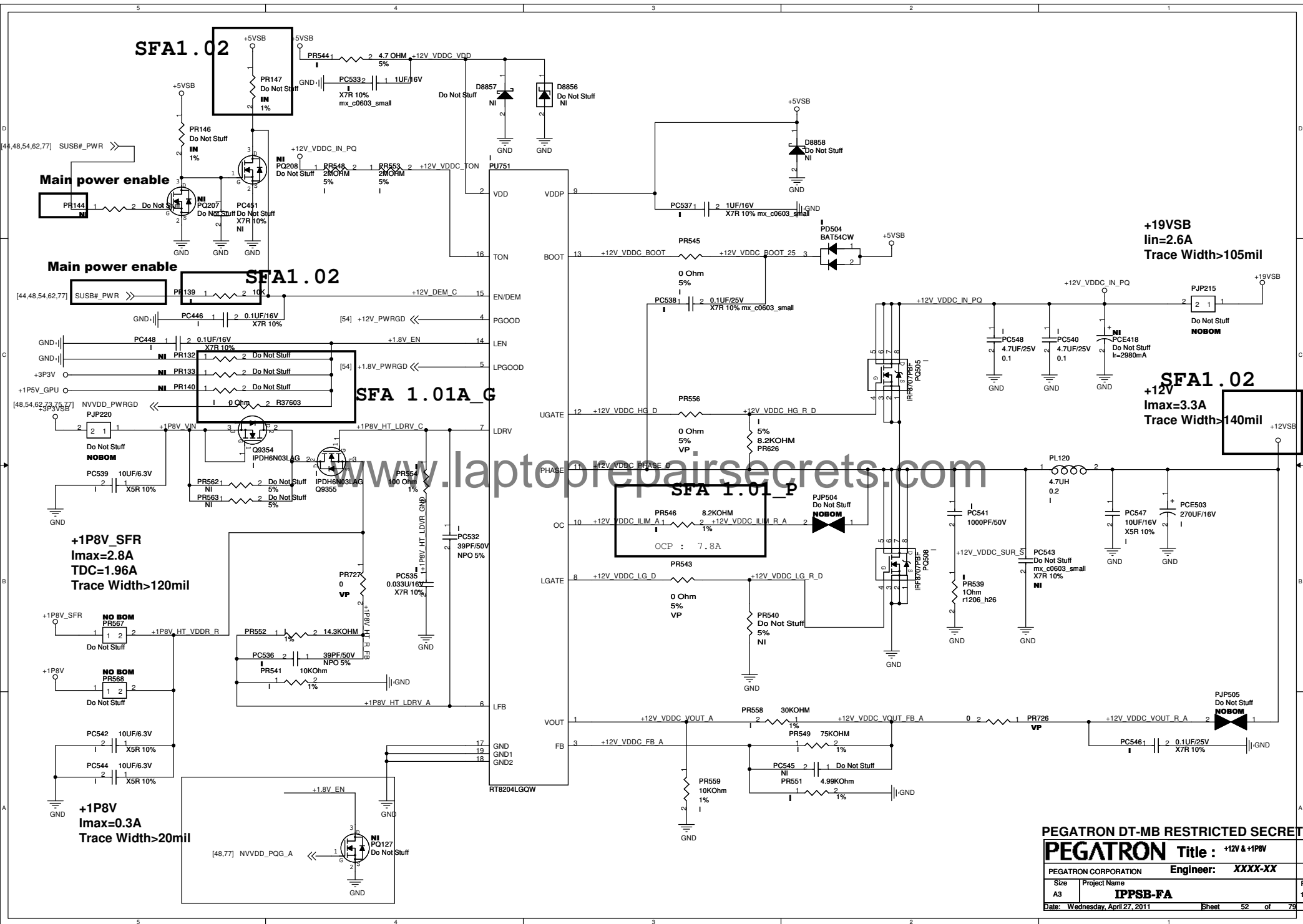
+3P3VSB
 $I_{max}=16.63A$
 $TDC=11.65A$
 Trace Width>680mil

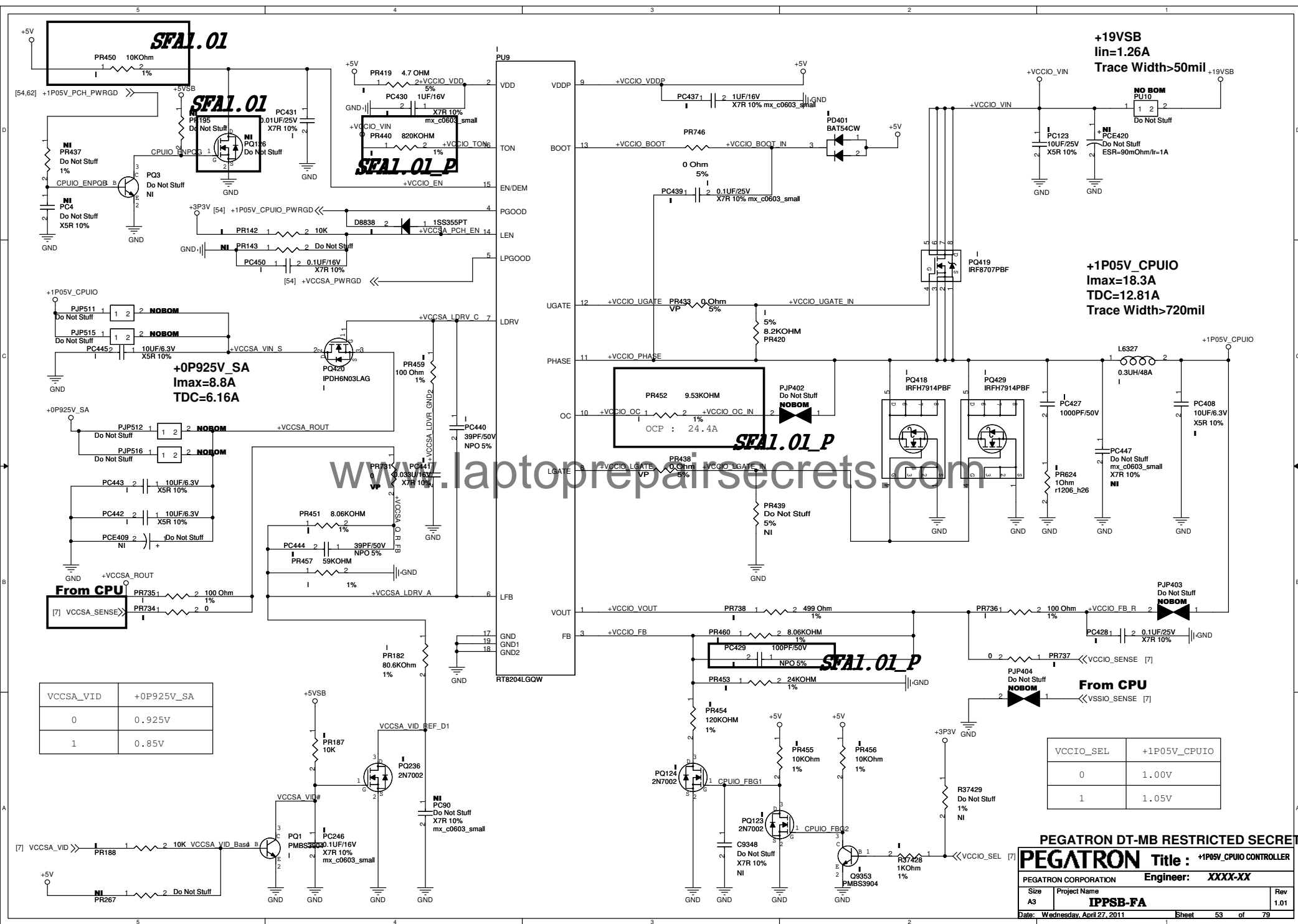


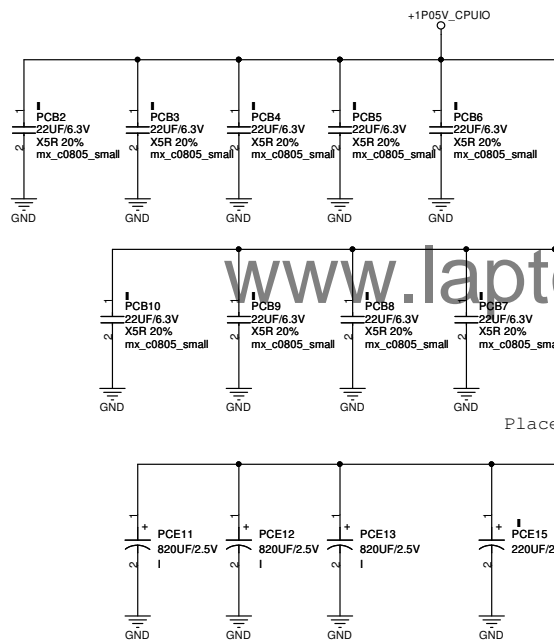
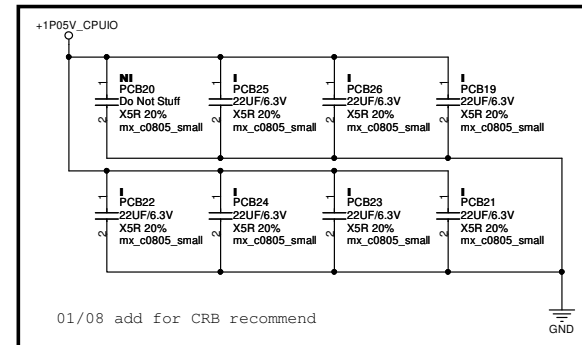
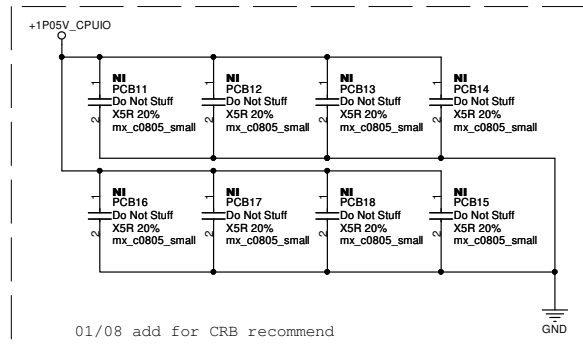




PEGATRON
1.01







VCCIO Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560uF	3	7mΩ	1.4nH	Output	Various. See layout figures	1
22uF 0805 X5R	9	5mΩ	0.55nH	Output	Inside processor socket cavity	1, 2, 3
0805 placeholders	16				Backside	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : 1P05V_CPUIO CAP

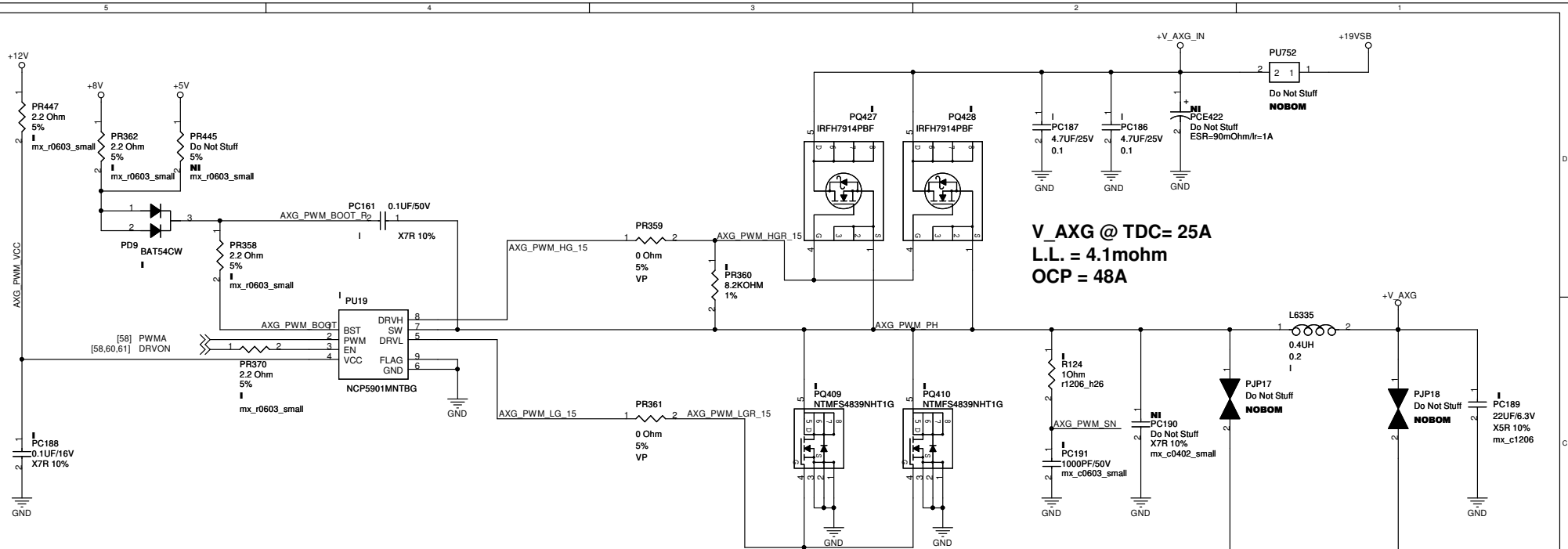
PEGATRON CORPORATION Engineer: XXXX-XX

Size Project Name

A3 IPPSB-FA Rev 1.01

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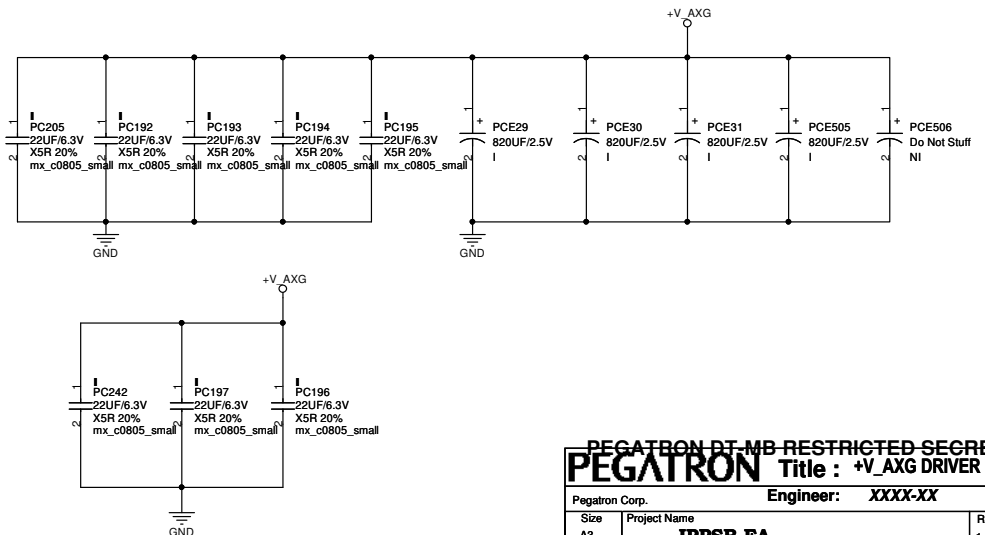
www.laptoprepairsecrets.com

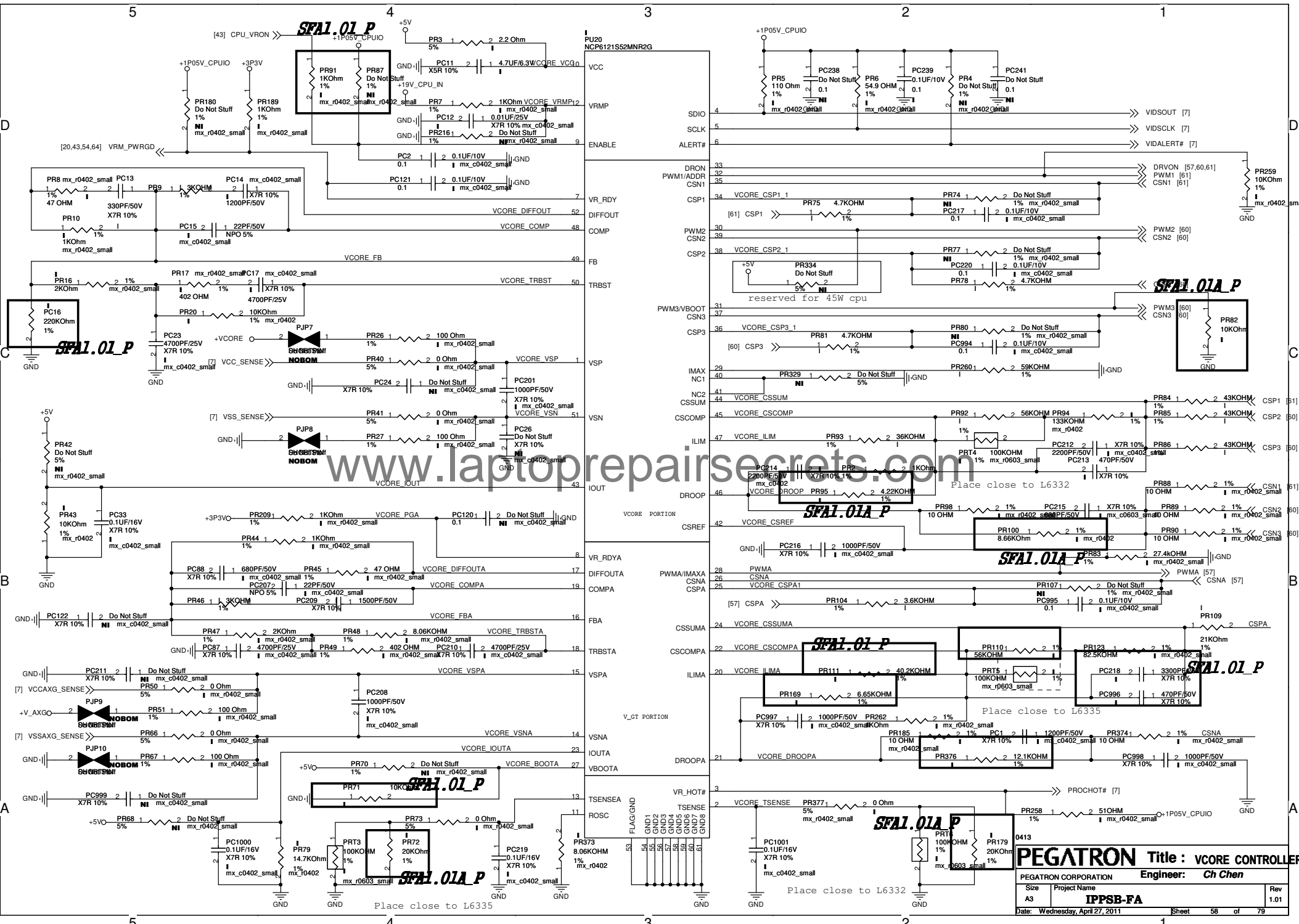
Output CAP

Table 30-4. VCCAXG Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	East of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	6	5mΩ	0.55nH	Output	4 - inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2, 3
4.7µF X5R	3	7mΩ	0.6nH	Input		1

PL-CAP *4
MLCC *6



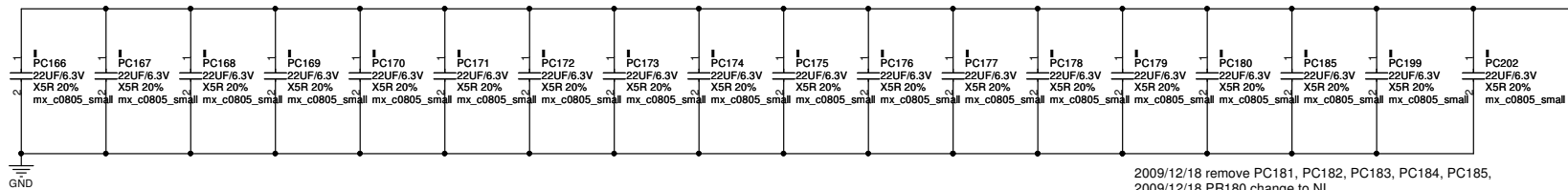
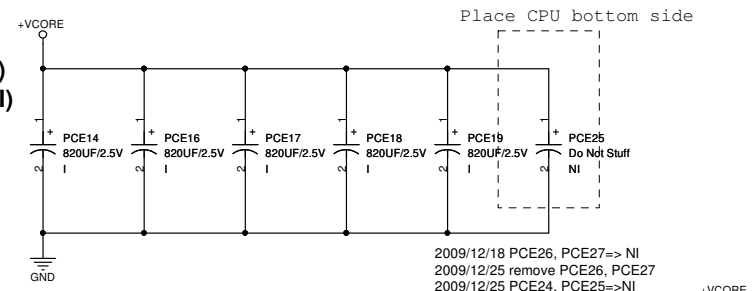


Output CAP

Table 30-2. Decoupling Requirements

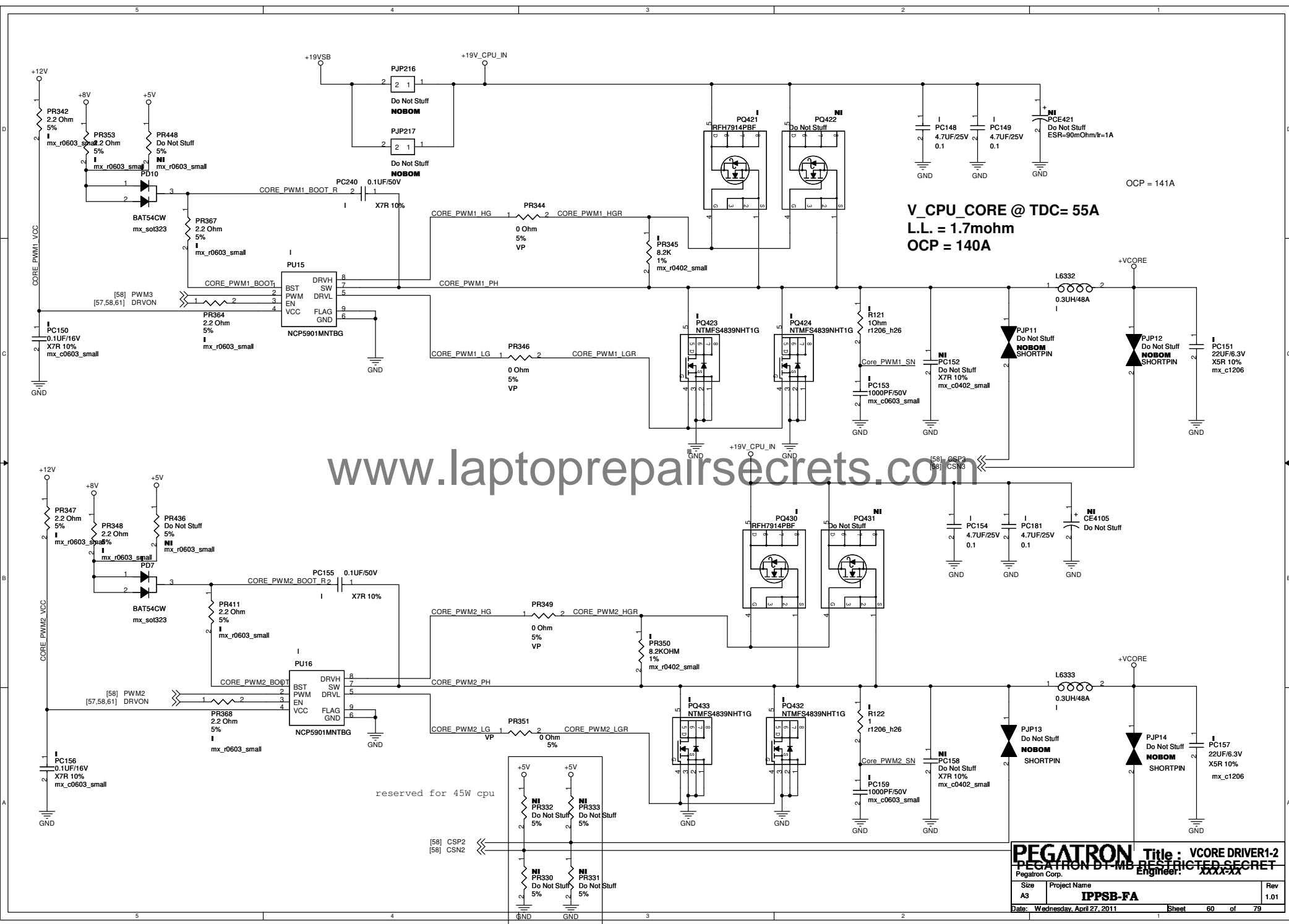
Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2, 3
Aluminum Electrolytic 390µF	4	51mΩ	6.1nH	Input		1
4.7µF X5R	9	7mΩ	0.6nH	Input		1

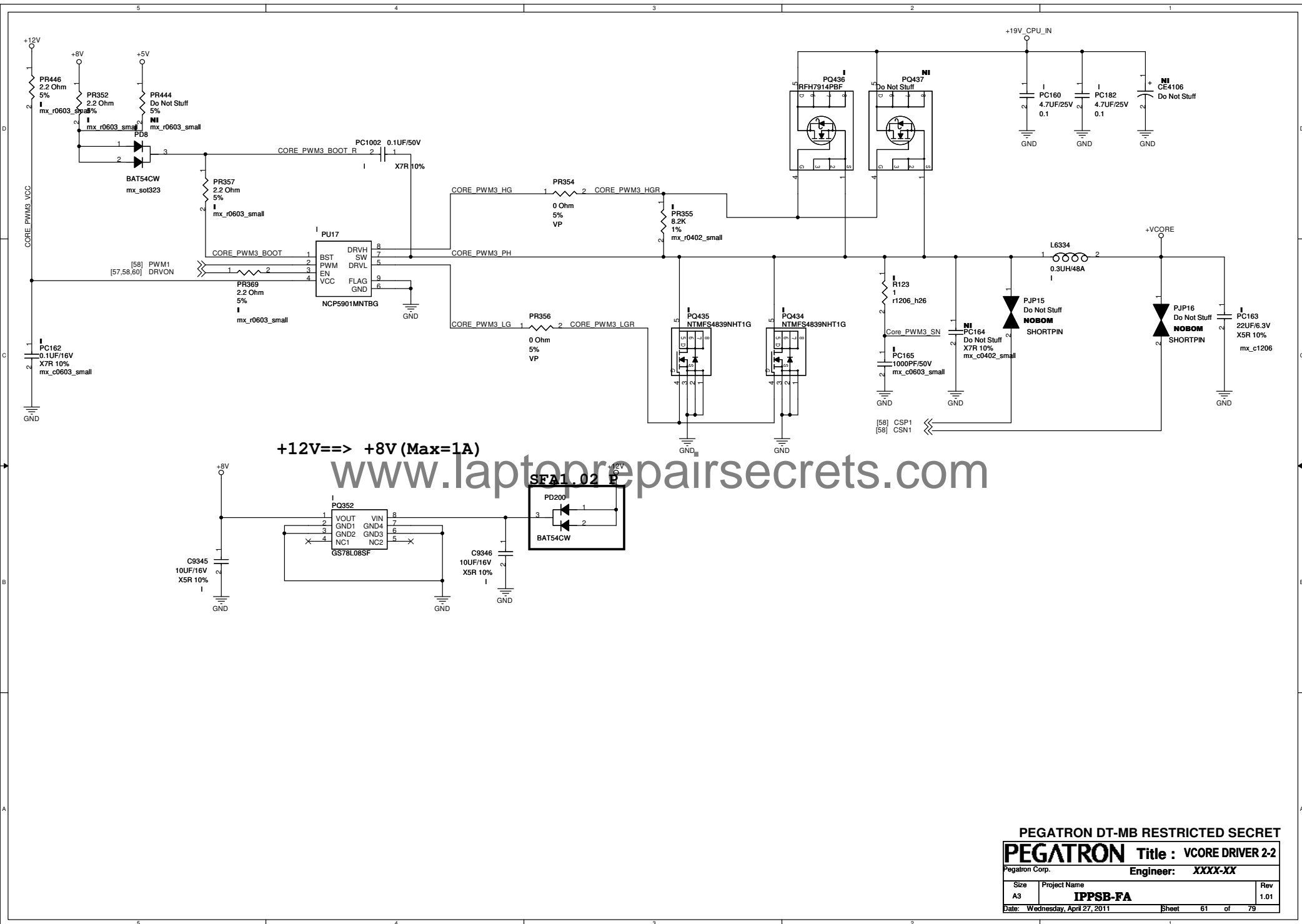
PL-CAP *4 +2(NI)
MLCC *18 +3(NI)



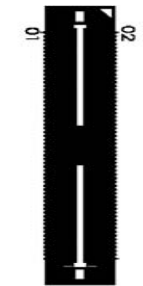
2009/12/18 remove PC181, PC182, PC183, PC184, PC185,
2009/12/18 PR180 change to NI
2009/12/21 PR180 change to I
2009/12/21 add PC185, PC199
2009/12/25 add PC200, PC201, PC202,
2009/01/09 remove PC200, PC201

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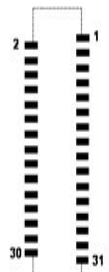




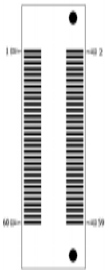
INTEL PCH XDP DEBUG PORT



TOP SIDE VIEW

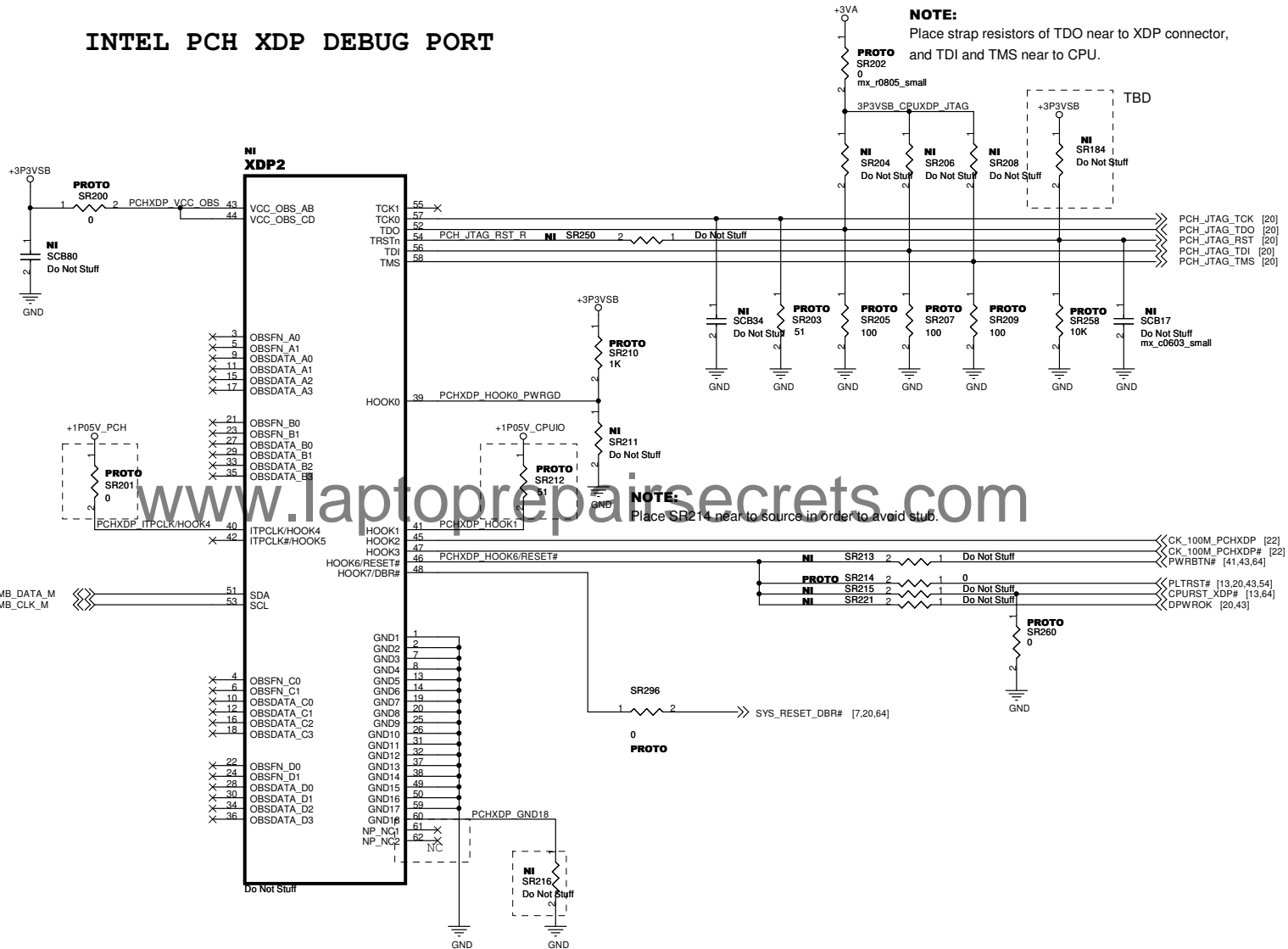


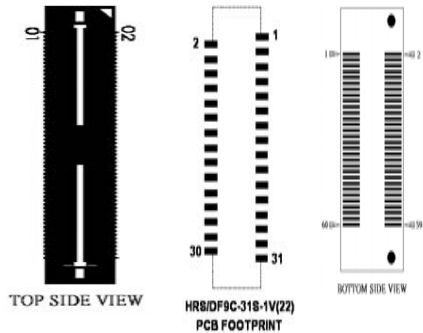
HR8/DF9C-31S-1V(22)
PCB FOOTPRINT



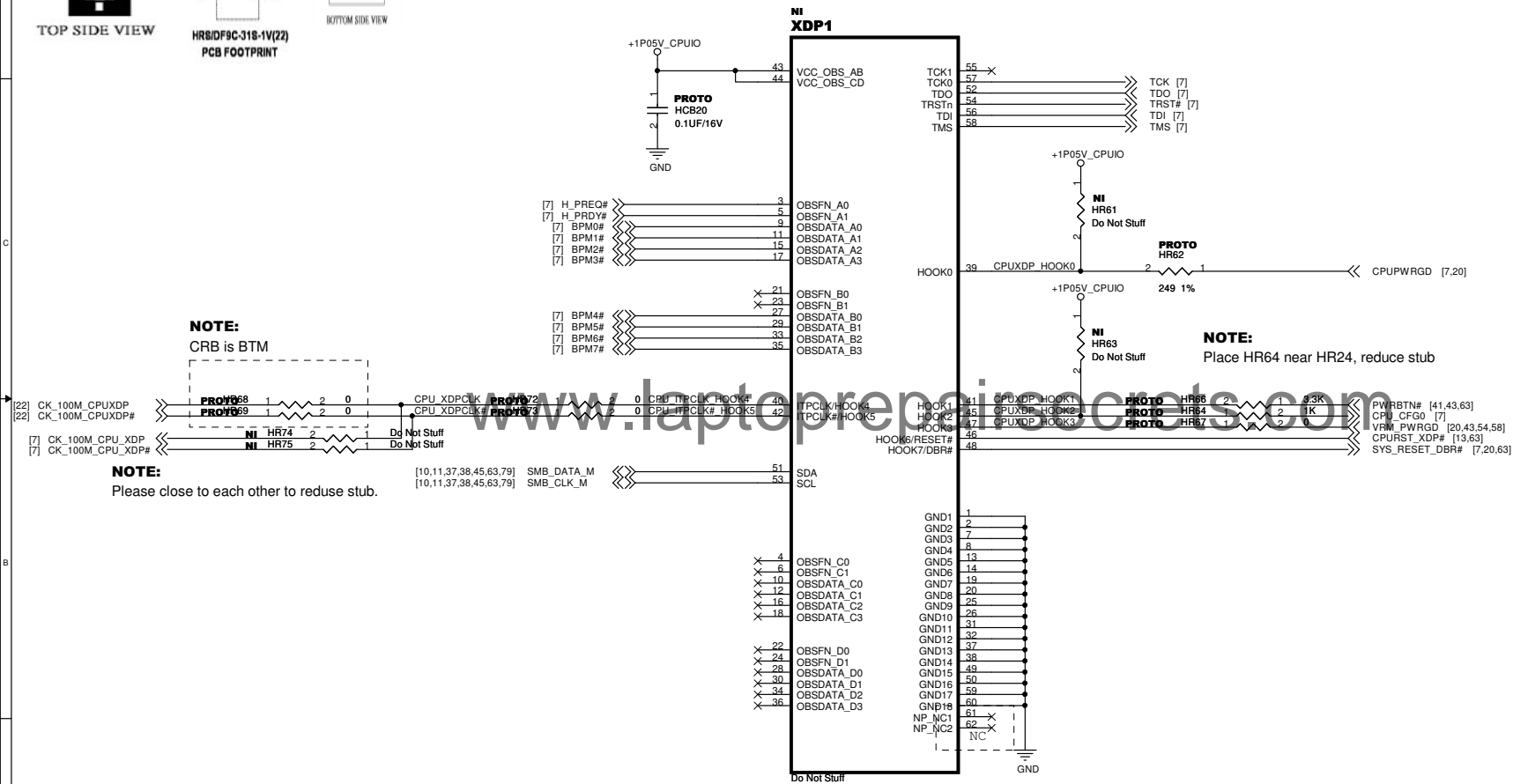
BOTTOM SIDE VIEW

[10,11,37,38,45,64,79] SMB_DATA_M
[10,11,37,38,45,64,79] SMB_CLK_M





INTEL CPU XDP DEBUG PORT



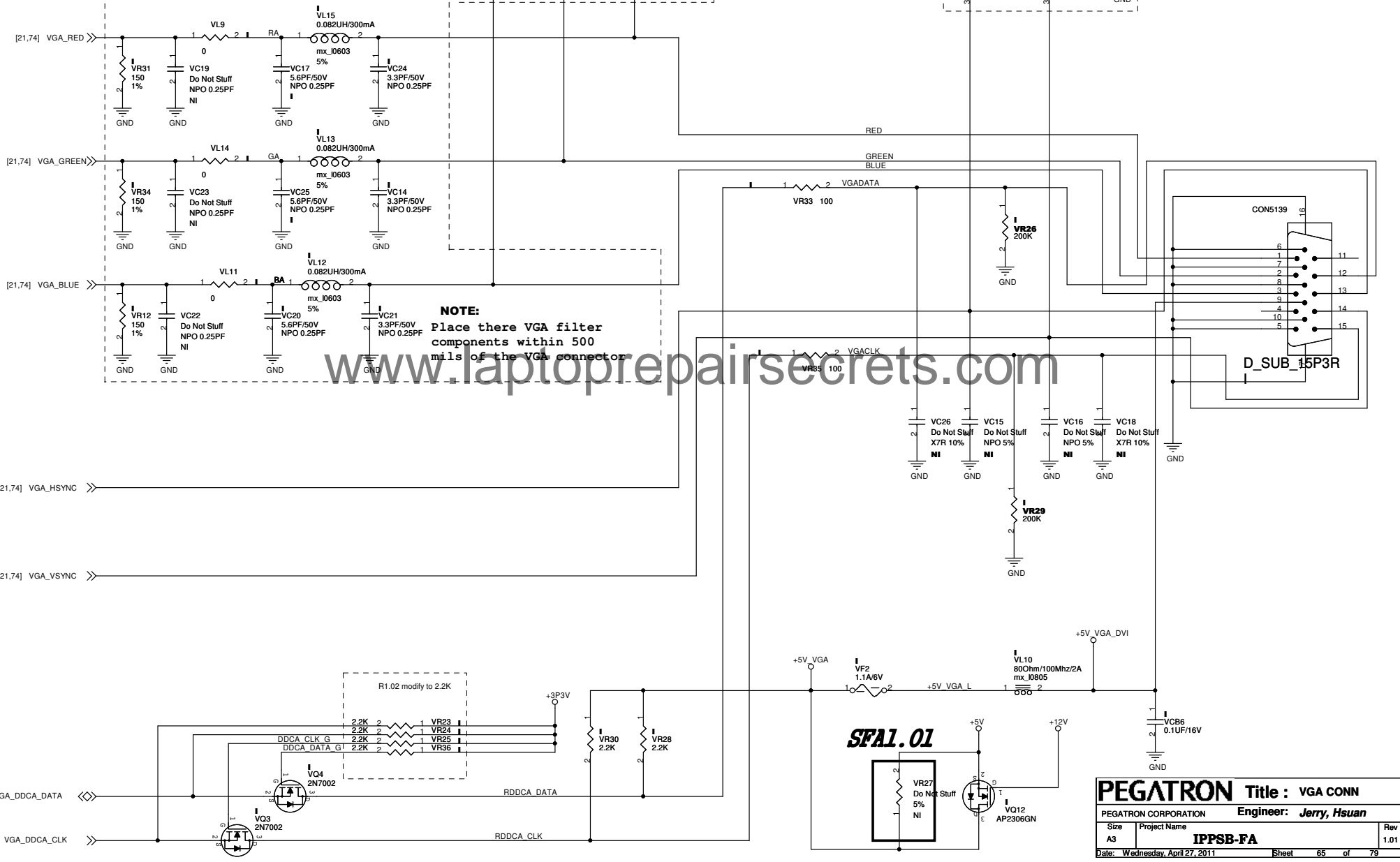
REGATRON DT-MB RESTRICTED SECRET

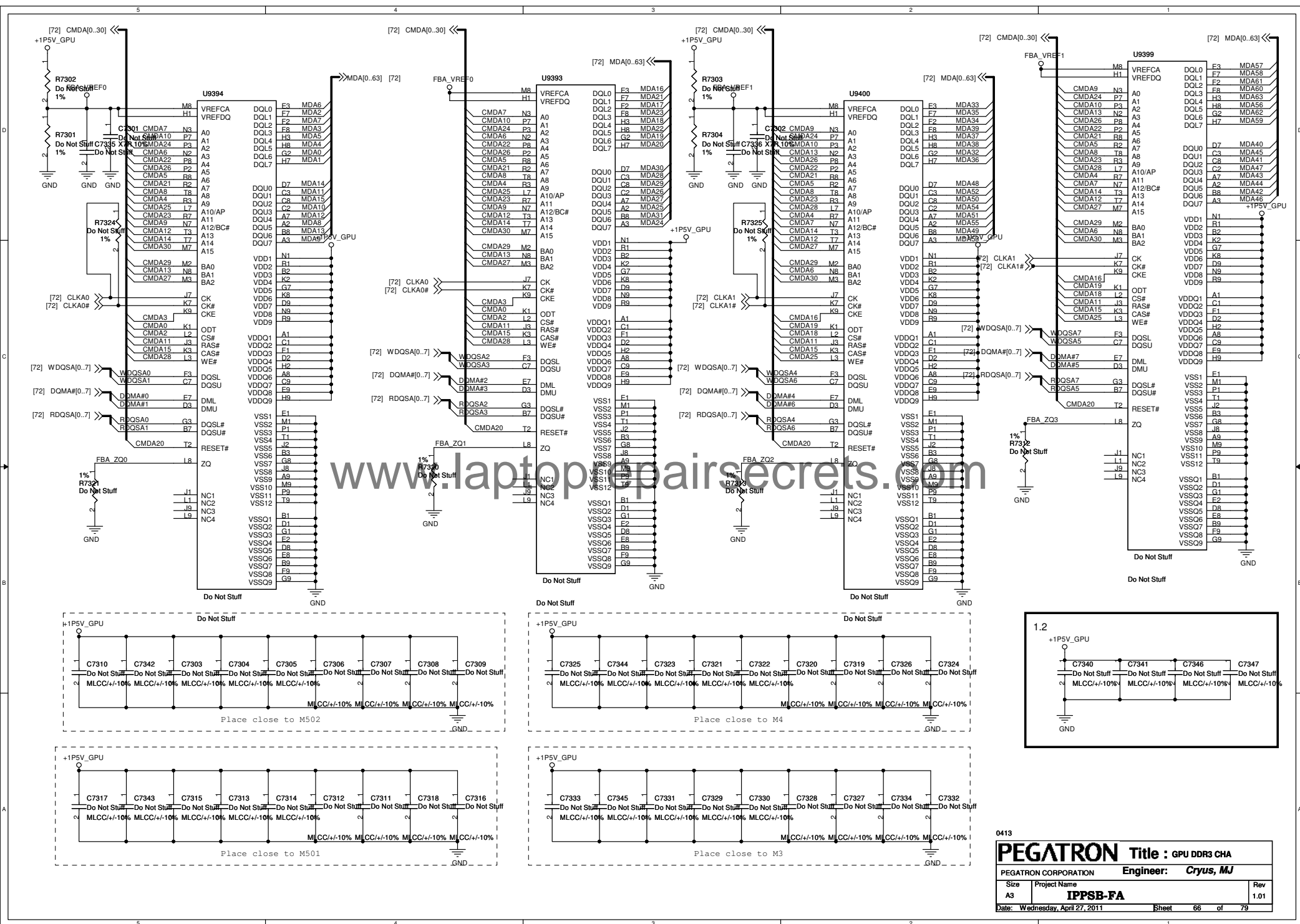
PEGATRON		Title : CPU XDP DEBUG	
PEGATRON CORPORATION		Engineer: XXXX-XX	
Size A3	Project Name IPPSB-FA		Rev 1.01
Date: Wednesday, April 27, 2011		Sheet 64 of 79	

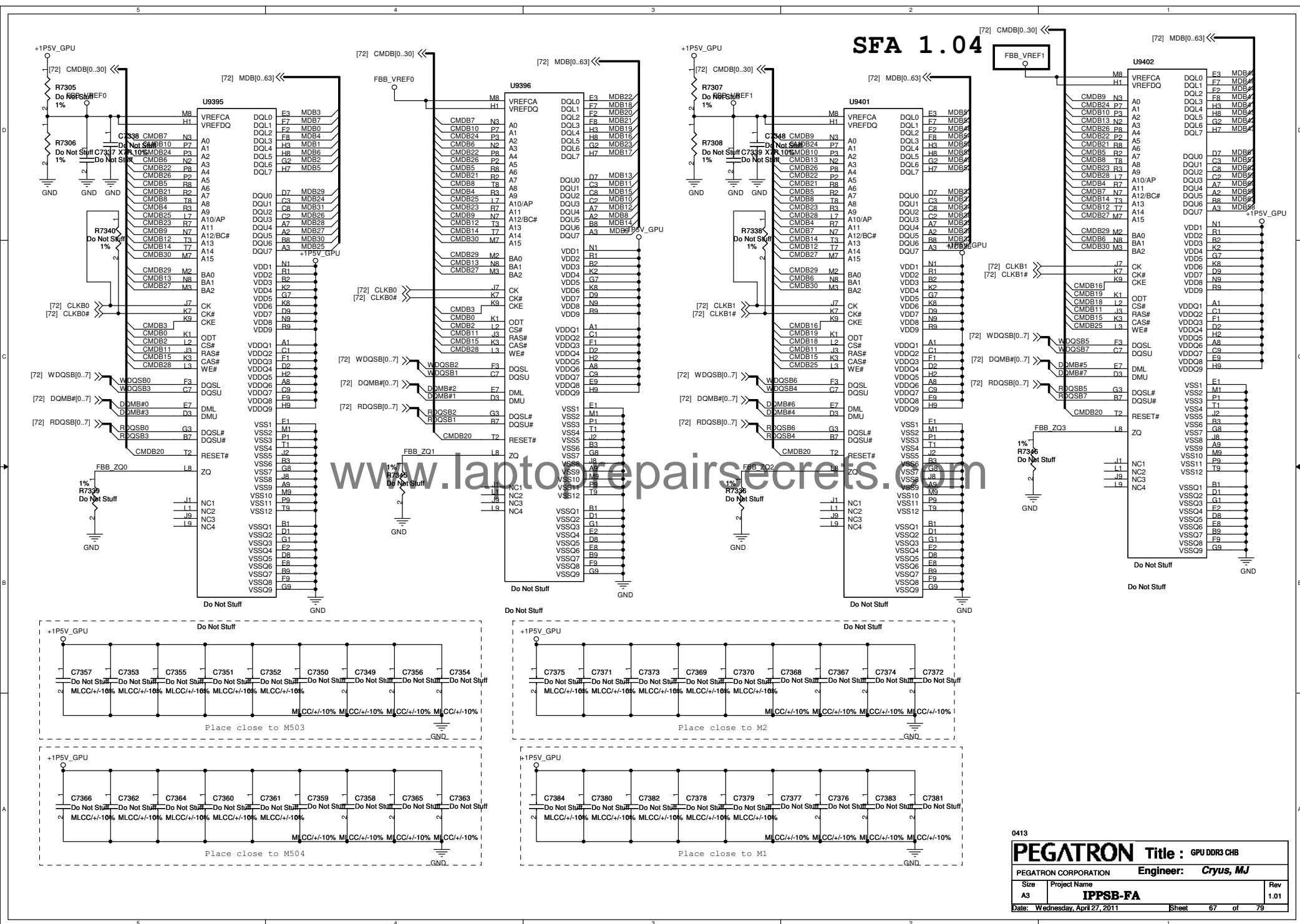
整份新增修改

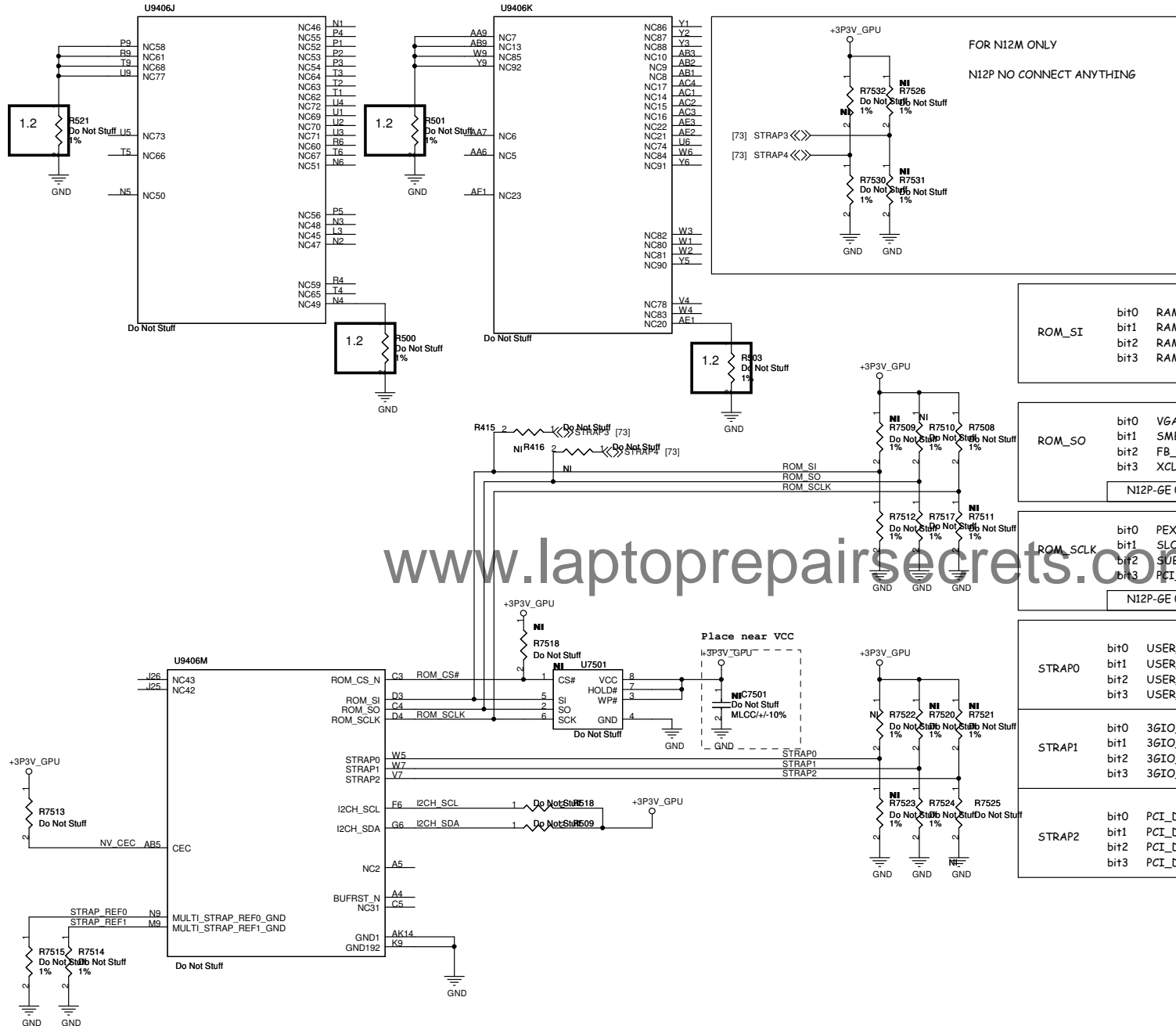
Install the VD1/VD2/VD3/VD4/VD5 diode to prevent from ESD issue

NOTE:









FOR NI2M ONLY
NI2P NO CONNECT ANYTHING

bit	Parameter	Value
bit0	RAM_CFG_0	1Gb (64Mx16 8pcs)
bit1	RAM_CFG_1	RAM_CFG[3:0] Definitions
bit2	RAM_CFG_2	0x2: Hynix => H5TQ1663BFR-12C
bit3	RAM_CFG_3	0x3: Samsung => K4W161646E-HC12

0x0010 : 15K PD

bit	Parameter	Value
bit0	VGA_DEVICE	1: VGA Device (default class code 300h)
bit1	SMB_ALT_ADDR	0: 0x9E (default)
bit2	FB_O_BAR_SIZE	0: 256MB (default)
bit3	XCLK_417	0: 277M Hz (default)

NI2P-GE 0x0001 : 10K PD NI2M-GS 0x1001 : 10K PU **different**

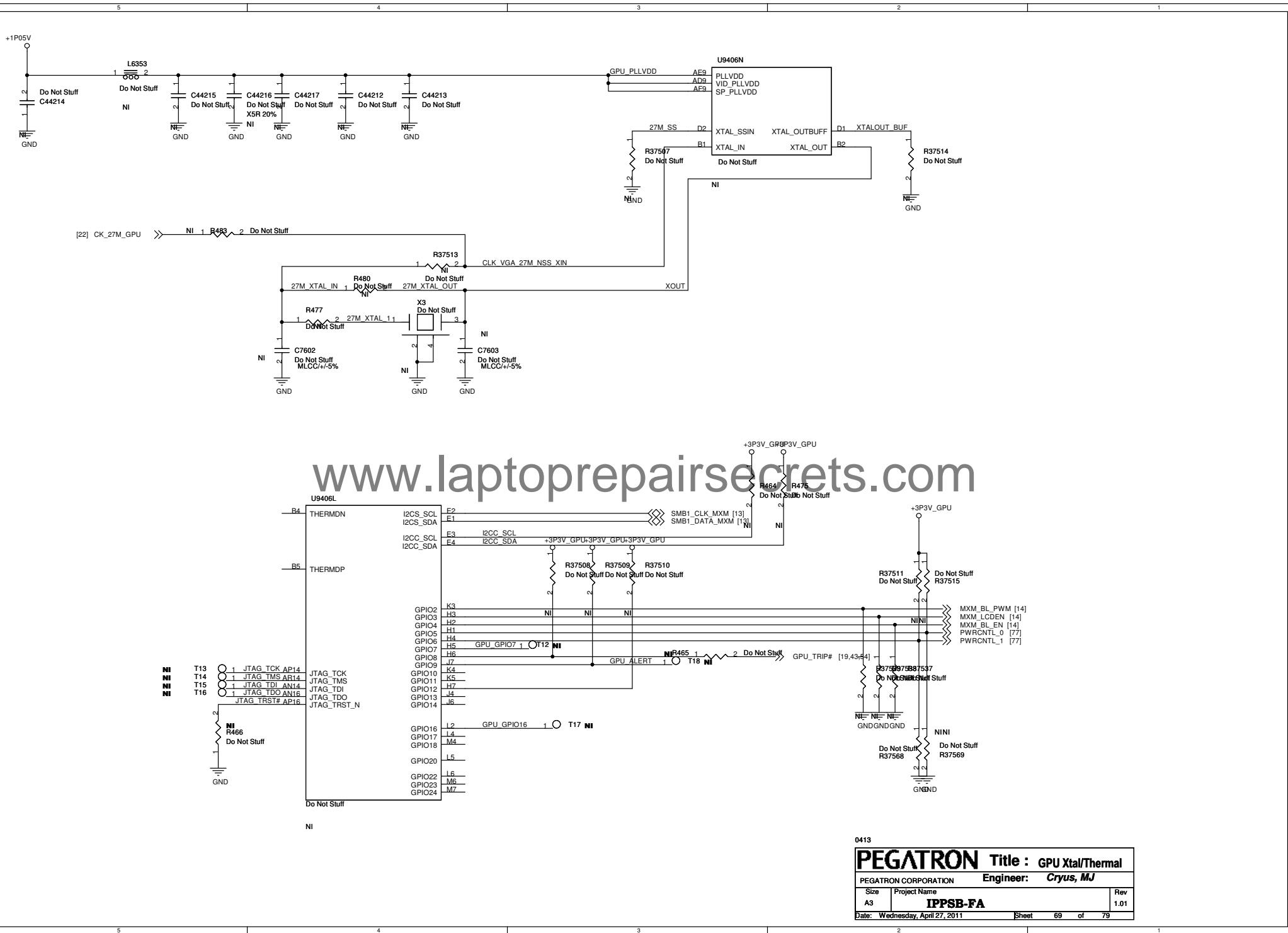
bit	Parameter	Value
bit0	PEX_PLL_EN_TERM	0: Disable (default)
bit1	SLOT_CLK_CONFIG	0: GPU & MCH not share common reference clock
bit2	SUB_VENDER	0: no vidio BIOS ROM
bit3	PCI_DEVID_4	1: PCI_DevID[4] => 0x0DFE bit 4 = 1

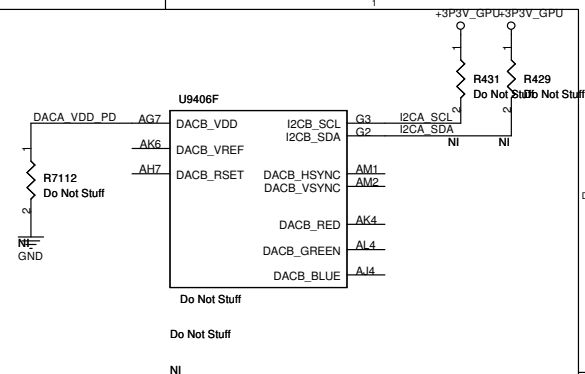
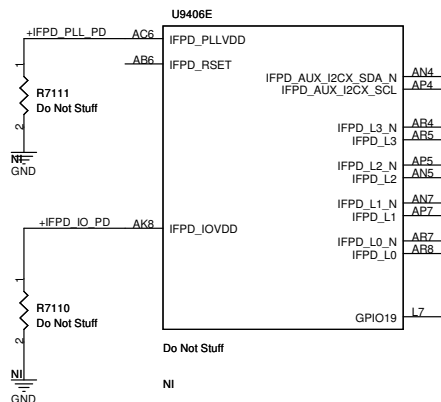
NI2P-GE 0x1110 : 35K PU NI2M-GS 0x1100 : 25K PU **different**

bit	Parameter	Value
bit0	USER_BIT0	0x0000 : 5K PD (Panels select Default 0x0000)
bit1	USER_BIT1	
bit2	USER_BIT2	
bit3	USER_BIT3	

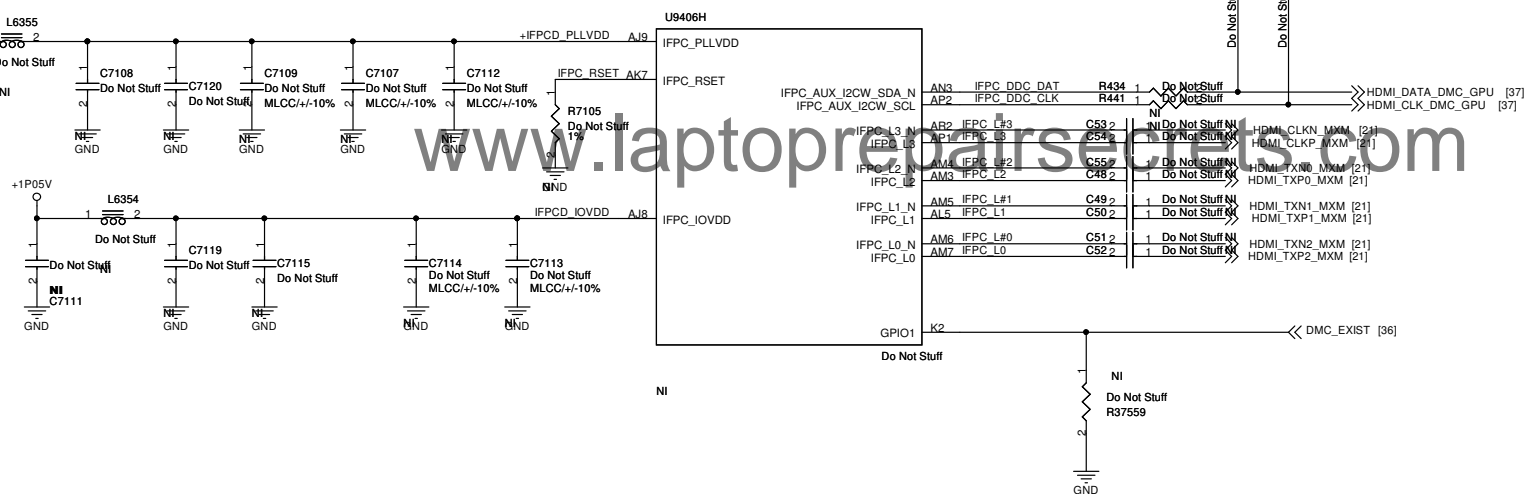
bit	Parameter	Value
bit0	3GIO_PADC6_LUT_ADR0	0x6 : 35k PD (PCIE swing default)
bit1	3GIO_PADC6_LUT_ADR1	
bit2	3GIO_PADC6_LUT_ADR2	
bit3	3GIO_PADC6_LUT_ADR3	

bit	Parameter	Value
bit0	PCI_DEVID_0	NI2P-GE 0x0101 : 30K PD NI2M-GS 0x0100 : 30K PD
bit1	PCI_DEVID_1	
bit2	PCI_DEVID_2	
bit3	PCI_DEVID_3	





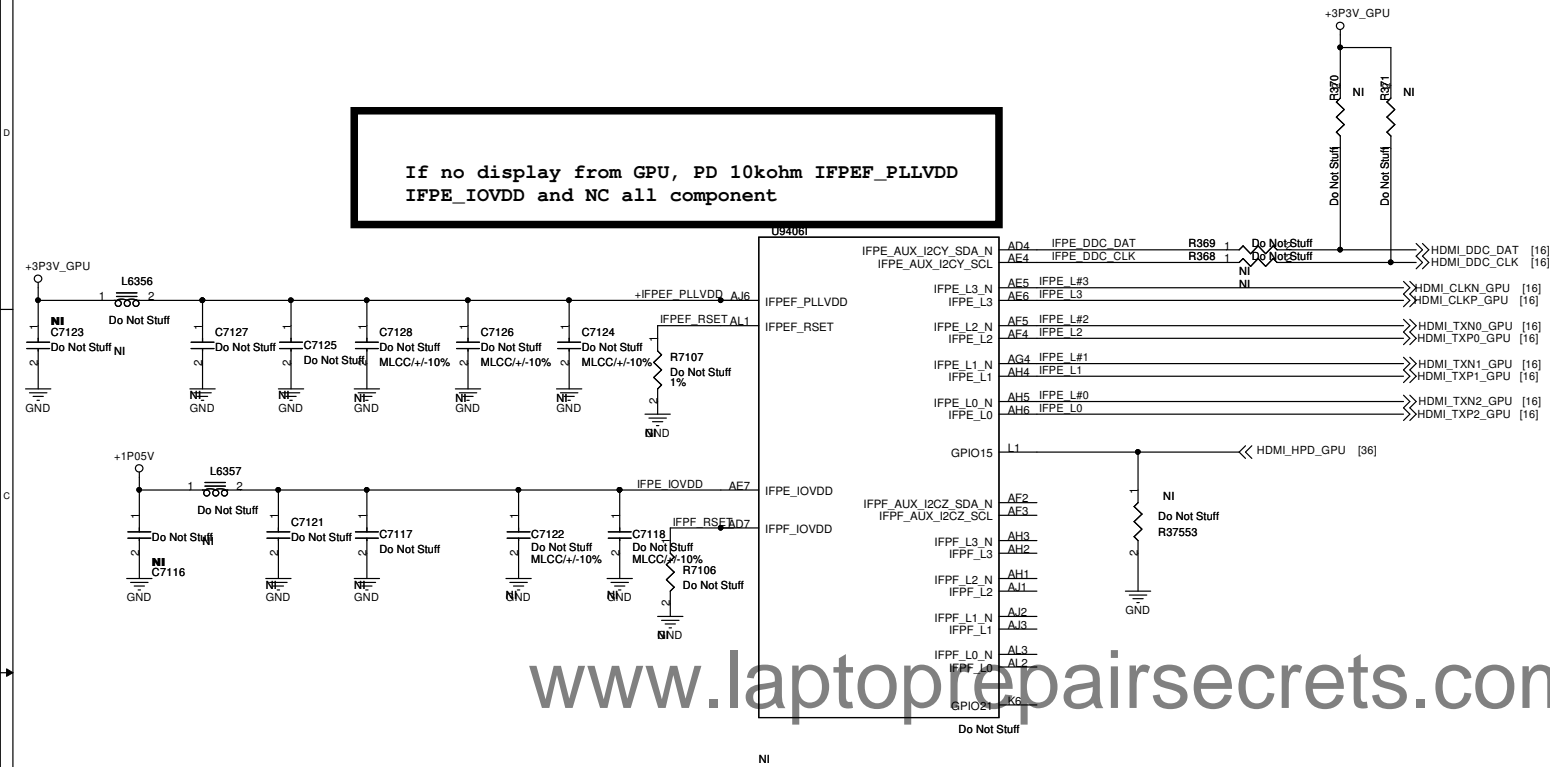
If no display from GPU, PD 10kohm IFPC_PLLVDD
IFPC_IOVDD and NC all component



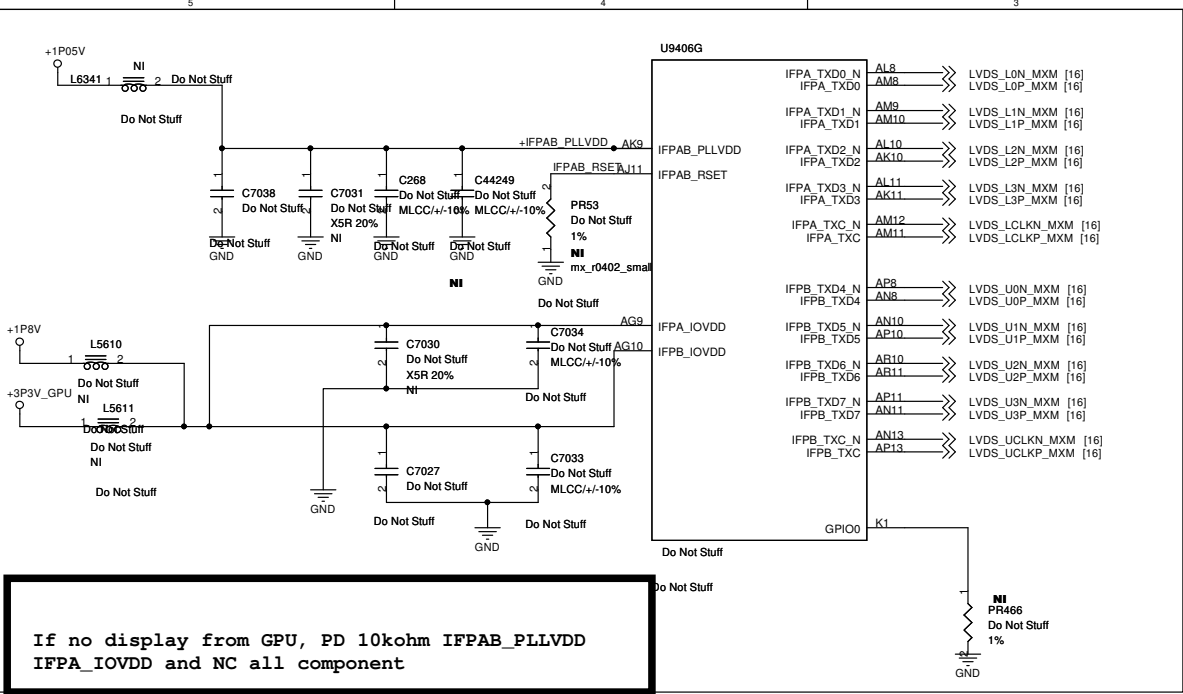
0413

PEGATRON		Title : GPU HDMI DMC	
PEGATRON CORPORATION		Engineer: Cryus, MJ	
Size A3	Project Name IPPSB-FA	Rev 1.01	
Date: Wednesday, April 27, 2011		Sheet	70 of 79

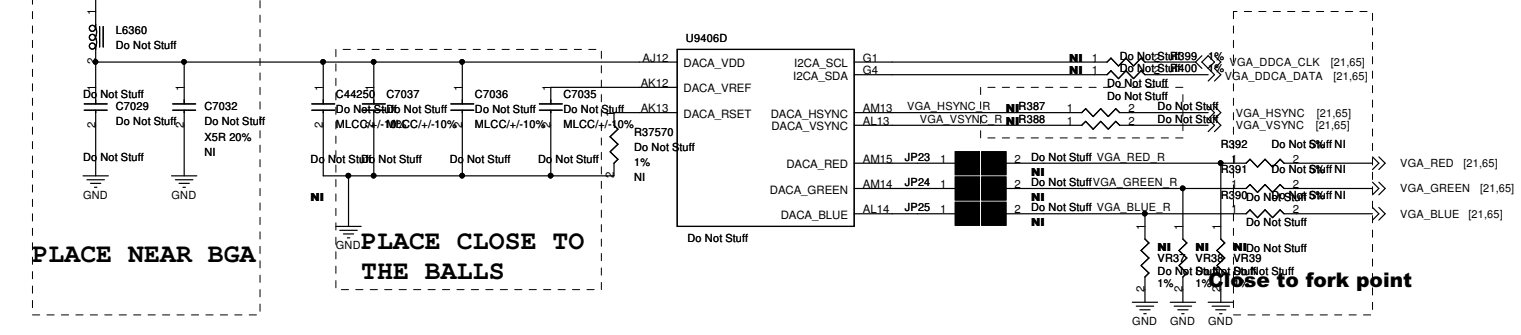
If no display from GPU, PD 10kohm IFPEF_PLLVDD
IFPE_IOVDD and NC all component



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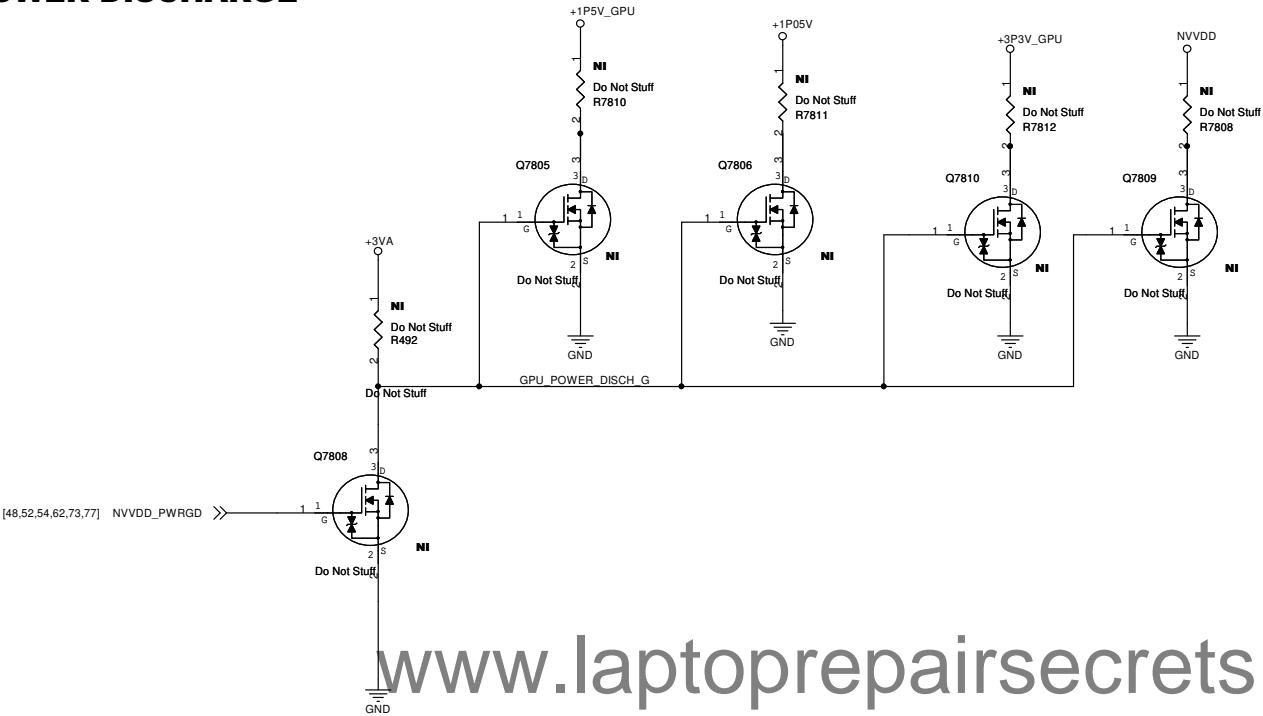
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If no display from GPU, PD 10kohm DACA_VDD ,PU 2.2kohm to +3P3V I2CA_SCL I2CA_SDA and NC all component

PLACE CLOSE TO BALLS

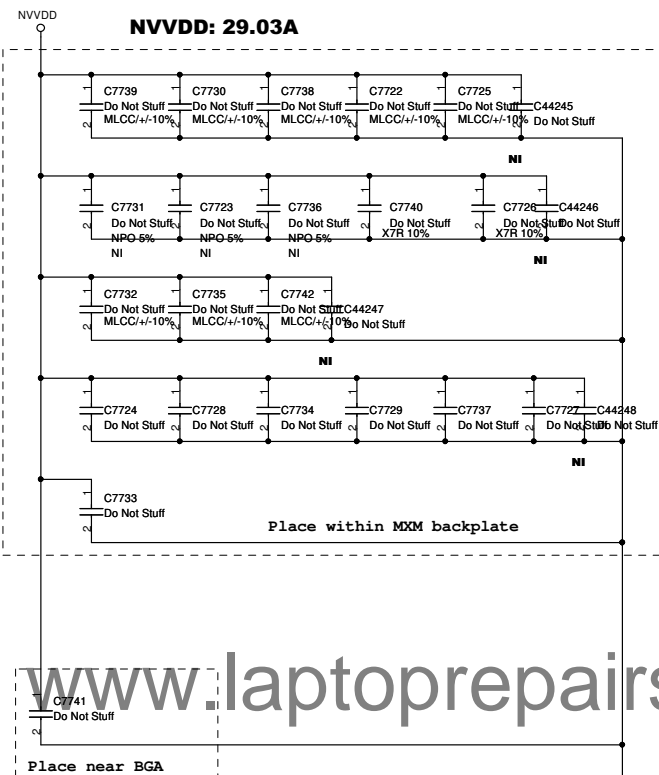
GPU POWER DISCHARGE



12/28 新增
01/07 修改

U9406P		
AB11	VDD1	P21
AB13	VDD2	P23
AB15	VDD3	P25
AB17	VDD4	R11
AB19	VDD5	R12
AB21	VDD6	R13
AB23	VDD7	R14
AB25	VDD8	R15
AC11	VDD9	R16
AC12	VDD10	R17
AC13	VDD11	R18
AC14	VDD12	R19
AC15	VDD13	R20
AC16	VDD14	R21
AC17	VDD15	R22
AC18	VDD16	R23
AC19	VDD17	R24
AC20	VDD18	R25
AC21	VDD19	T12
AC22	VDD20	T14
AC23	VDD21	T16
AC24	VDD22	T18
AC25	VDD23	T20
AD12	VDD24	T22
AD14	VDD25	V11
AD16	VDD26	V13
AD18	VDD27	V15
AD22	VDD28	V17
AD24	VDD29	V19
L11	VDD30	V21
L12	VDD31	V23
L13	VDD32	V25
L14	VDD112	W11
L15	VDD34	W13
L16	VDD35	W15
L17	VDD36	W17
L18	VDD37	W19
L19	VDD38	W21
L20	VDD39	W23
L21	VDD40	W25
L22	VDD41	Y12
L23	VDD42	Y14
L24	VDD43	Y16
L25	VDD44	Y18
M12	VDD45	Y20
M14	VDD46	Y22
M16	VDD47	Y24
M18	VDD48	
M20	VDD49	
M22	VDD50	
M24	VDD51	
P11	VDD52	
P13	VDD53	
P15	VDD54	
P17	VDD55	
P19	VDD56	

Do Not Stuff



U9406O		
AA11	GND2	E15
AA12	GND3	E18
AA13	GND4	E24
AA14	GND5	E27
AA15	GND6	E30
AA16	GND7	E6
AA17	GND8	E9
AA18	GND9	E2
AA19	GND10	F31
AA2	GND11	F34
AA20	GND12	F5
AA21	GND13	J2
AA22	GND14	J31
AA23	GND15	J34
AA24	GND16	J5
AA25	GND17	L9
AA34	GND18	M11
AA5	GND19	M13
AB12	GND20	M15
AB14	GND21	M17
AB15	GND22	M19
AB16	GND23	M2
AB20	GND24	M21
AB22	GND25	M23
AB24	GND26	M25
AC3	GND27	M31
AD11	GND28	M34
AD13	GND29	M5
AD15	GND30	N11
AD17	GND31	N12
AD2	GND32	N13
AD21	GND33	N14
AD23	GND34	N15
AD25	GND35	N16
AD31	GND36	N17
AD34	GND37	N18
AD5	GND38	N19
AE11	GND39	N20
AE12	GND40	N21
AE13	GND41	N22
AE14	GND42	N23
AE15	GND43	N24
AE16	GND44	N25
AE17	GND45	P12
AE18	GND46	P16
AE19	GND47	P18
AE20	GND48	P20
AE21	GND49	P22
AE22	GND50	P24
AE23	GND51	R2
AE24	GND52	R31
AE25	GND53	R34
AG2	GND54	R5
AG31	GND55	T11
AG34	GND56	T13
AG5	GND57	T15
AK2	GND58	T17
AK31	GND59	T19
AK34	GND60	T21
AK5	GND61	T23
AL12	GND62	T25
AL15	GND63	U11
AL18	GND64	U12
AL21	GND65	U13
AL24	GND66	U14
AL27	GND67	U15
AL30	GND68	U16
AL6	GND69	U17
AL9	GND70	U18
AN2	GND71	U19
AN34	GND72	U20
AP12	GND73	U21
AP15	GND74	U22
AP18	GND75	U23
AP21	GND76	U24
AP24	GND77	U25
AP27	GND78	V12
AP3	GND79	V14
AP30	GND80	V16
AP33	GND81	V18
AP6	GND82	V2
AP9	GND83	V20
B12	GND84	V22
B15	GND85	V24
B21	GND86	V31
B24	GND87	V5
B27	GND88	V9
B3	GND89	Y11
B30	GND90	Y13
B33	GND91	Y15
B6	GND92	Y17
B9	GND93	Y19
C2	GND94	Y21
C34	GND95	Y23
E12	GND96	Y25

Do Not Stuff

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : GPU POWER&GND

PEGATRON CORPORATION		Engineer: Cryus, MJ	
Size	Project Name	Rev	
A3	IPPSB-FA	1.01	
Date: Tuesday, April 26, 2011		Sheet 76 of 79	

